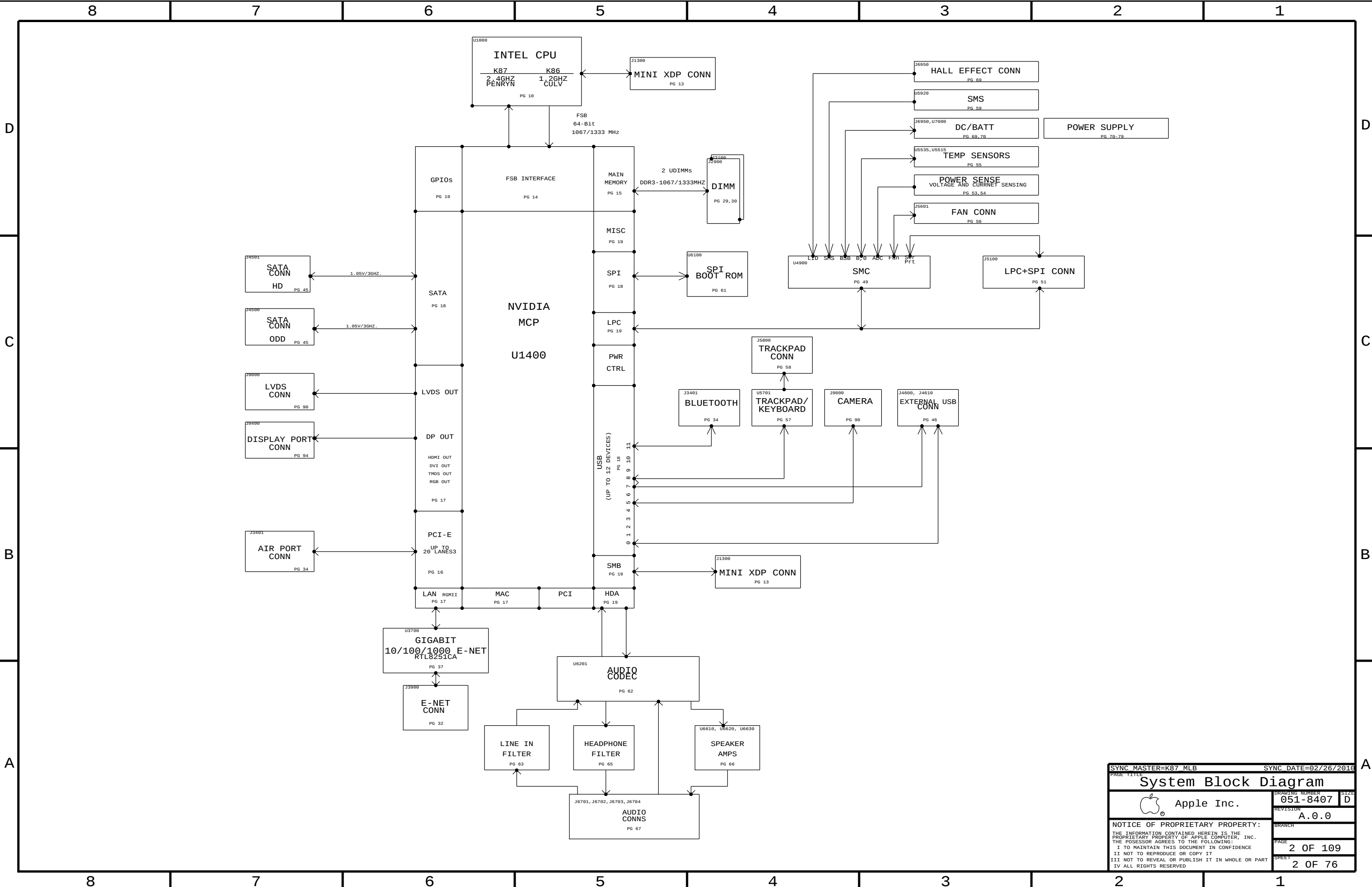




SYNC MASTER=K87 MLB

SYNC DATE=02/26/2010

System Block Diagram

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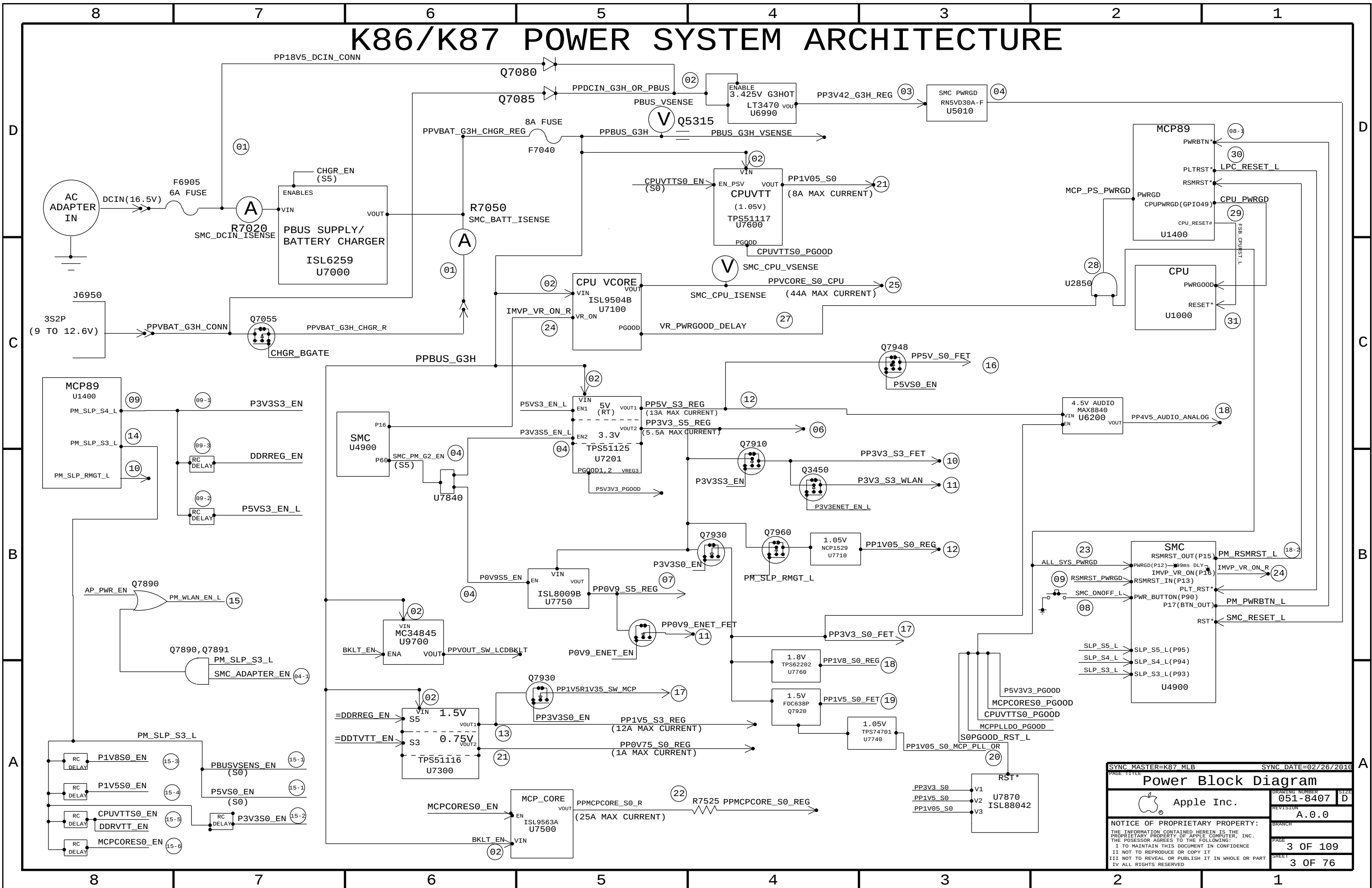
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K86/K87 POWER SYSTEM ARCHITECTURE



SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE		Power Block Diagram	
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BOM Variants

Bar Code Labels / EEE #'s

Development BOM

Development BOM

Part Substitutions (differences with K6/K69)

BOM Groups (always-present)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0125	1	RES, MTL FILM, 1/16W, 113 OHM, 1, 0402, SMD, LF	R5714		LED:K86_K87

BOM Groups (project phase-dependent)

Module Parts

K86/K87 BOARD STACK-UP

```

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

```

TOP	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

Alternate Parts

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PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER 051-8407	SIZE D
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Revision History

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

10/1/2009:INITIAL RELEASE 0.0.1.
- REPLACES SYNC'ED FROM K84
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

2009-12-03: Proto 0 release 1.0.0

2009-12-04: 1.1.0
csa 3: Deleted CPU block text to include CPU description for both K86 and K87
csa 3: Updated text note to include "K86" in title
csa 4: Added BOM entry under Module Parts table to include CULV processor (337S3779) to minimize delta on this page between K86 and K87 per Diana

2009-12-07: 1.2.0
csa 74: Comment value changes per Leo (Intersil):
R7417 from 8.36k => 6.34k 1% (114S0296)
C7434 152S0102
Implemented different stuffing options for 1-phase vs 2-phase:
Added IMVP6.2PHASE to the following components:
R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413
Added BOM table to insert the following APNs for IMVP6.1PHASE:
R7417 = 7.88k 1% (114S0304)
C7428 = 0.22uF 10% (132S0102)
R7411 = 255 1% (114S0160)
C7406 = 470nF 10% (132S0120)
R7414 = 97.6k 1% (114S0410)
C7414 = 1000pF 10% (132S0845)
C7413 = 1000pF 5% (131S1027)
Updated table to add new values for 1phase (PWM freq., Max current, Load line)
csa 6: STILL NEED TO UPDATE VALUE OF C7428!

2009-12-08: 1.3.0
csa 45: Added passive deemphasis to SATA HDD D2R lines:
Added R4585, R4586 (51.1 ohm, 1% 114S0093) and OMITTED
C4585, C4586 (100pF, 5% 131S0099) and NOSTUFFED
Added BOM table to stuff 0-ohms until we get go-ahead for filter

2009-12-08: 1.4.0
csa 8: Deleted net properties for the following nets:
=PP3V3_S0_CPUVTT15MS'
=PP5V_S0_HDD'
=PP5V_S0_MCPREG'
=PP1V05_S0_MCP_AVDD_UF'
=PP5V_S0_MCP_8'
=PP3V3_S0_PMRCTL'
=PP3V3_S0_DPDOWN'
csa 34: Deleted net properties for =PP3V3_S3_WLAN
csa 74: Changed C7434 from NOSTUFF to IMVP6.2PHASE per Intersil
Added IMVP6.2PHASE to R7413 per Intersil
Changed C7428 from 0.47uF to 0.33uF (132S0101) per Intersil
Changed component color to green
Cosmetic cleanup
csa 90: Deleted net properties for =PP5V_S3_CAMERA
csa 98: Deleted net properties for =PPBUS_S0_LCDCLKLT'
csa 108: Deleted NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N

2009-12-09: 1.5.0
multiple: Added parentheses for SYNC_DATE property on all pages that have broken sync.
csa 4: Deleted entry in Module Parts table for R6612, R6613, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers
csa 69: Changed J6955 symbol to K87 Hall effect assembly (33S08114)

2009-12-10: 1.6.0
csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector

2009-12-11: 1.7.0
csa 45: Added PLACEMENT NOTE for passive deemphasis circuit.
csa 74: Changed 1PHASE BOM table to correctly call out 132S0080 (0.22uF) instead of 0.022uF

2009-12-16: 1.8.0
*** Resynced all synced pages and picked up the following (change notes from T27):
csa 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). <rdar://7416025> Ensure USB_EXTB is on ports 8-11 (NVRN-612340)
csa 20: T27: Changed USB_REBIAS from 931-ohms to 887-ohms per DG v1.3 (pg. 18). <rdar://7459260> Design Guide v1.3 updates
csa 29: T27: Added LKPLUS_WAIVE properties to dismiss false errors (pg. 20). <rdar://7368523> Task: Wipe false CheckPlus errors
*** Started syncing the following pages:
csa 29,31: Began syncing from T27 per <rdar://7424246 > BOM: K87 needs omit on J3100 and J2900 from T27
csa 54: T27: Added BOMPTIONS and APNs for Foxconn and Molex S0-DIMM connectors (pg. 29, 31).
C5490 changed from CAP 402-0.022UF,10%,10V,CEM-XSR to CAP 402-0.022UF,20%,10V,CEM
T27: Added LKPLUS_WAIVE properties to dismiss false errors (pg. 54).
T27: Added gain note for U5402 and SMC BAT1 sense (pg. 54).
csa 57: T27: Changed RC balance on BAT1 sense. Same time constant (pg. 54).
Began syncing from T27 per <rdar://7368523> T27 schematic bom option for R5714 & R5030 to keep K87 in sync
R5714 has BOMPTION LED:K6_K69, and we need to substitute a different part on csa 4
*** Made the following changes to follow T27 on the following unsynced pages:
csa 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <rdar://7459260 > Design Guide v1.3 updates
*** Other changes:
csa 4: Added BOM table to substitute in parts that have BOMPTION xxx:K6_K69 (to allow sync with T27)
Added R5714 (114S0125) to table with BOMPTION LED:K86_K87

2009-12-17: 1.9.0
csa 4: Added BOM table entry for MCP89-A02 per <rdar://7416058 > Task: Get part numbers for A02 rev.
csa 34: Changed K87_MCP_BOM group to call out MCP89-A02
Changed R3440 from A02 part to A02 (34S0811) per <rdar://7459498> BOM: APN updates for PFP1009 and SAK parts
Updated QLV text note for U3440 to match T27
Changed R3440 color to green, deleted WF text note about needing PU
csa 72: Changed L7200 from 152S0093 to 152S0778 per <rdar://problem//7347216> K69 L7200 combo footprint
Alternates table on csa 4 already has 152S0778 as alternate to 152S0693

2009-12-22: 1.10.0
csa 4: Per <rdar://problem//7473229> K86: Move to MCP83
Added BOM table entry for MCP83M (337S3876)
This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86
BOMPTION is MCP83M
Per <rdar://problem//7495072> K87: Call out LED:K86_K87 BOMPTION in the K87_MISC BOM group
Added LED:K86_K87 BOMPTION to the K87_MISC BOM group
Per <rdar://problem//7495116> K87: remove ON Semi alternate for Q2300 (376S0624)
Removed table entry that says 376S0609 is an alternate for 376S0624
Per <rdar://problem//7495021> K86/K87: Replace "S" APNs with "T" APNs for programmed SMC and BR
Changed BOMPTION to call out 376S0609 and 376S0624
Created SMC:PROG_K87 pointing to 341T0252 (SUBASSY, IC, SMC, K87)
Created SMC:PROG_K86 pointing to 340250 (SUBASSY, IC, SMC, K86)
Changed K87_PROGAPTS BOM group to point to SMC:PROG_K87
csa 69: Per <rdar://problem//7494087> K87: remove OMIT from J6955 and delete BOM table
Deleted BOM table for Hall effect assembly
Changed text note to say "HALL EFFECT ASSEMBLY"
Deleted OMIT BOMPTION from J6955
Added text note with part numbers for components of the assembly
Assembly APN: 33S08114
- BOM: 639-0680
- PCB: 839-2801
- MCO: 056-3515
- Conn APN: 518S0788

csa 74: Cosmetic change, moved R7413, C7406 BOMPTION label so they don't look like wire name
csa 78: Per <rdar://problem//7495068> K87: Add NOSTUFF to R7872 to disconnect U7870 from ALL_SYS_PWRGD
Changed BOMPTION for R7872 from S0P000_ISL to NOSTUFF

2010-01-06: 1.11.0
csa 7: Per <rdar://problem//7517432> K86/K87 functional net property needed on signals in schematics
Added the following functional test points under the J5100 LPC+SPI_CONN_FUNC_TEST group
LPCPLUS_GPTD
LPC_SERIALQ
SMC_TMS

2010-01-07: 1.12.0
csa 23: Per <rdar://problem//7519025> K86/K87: update all instances of 376S0786 schematic symbols
Updated Q2355 and Q2356 with new schematic symbols
Need to resync with T27 once the change has been made there
csa 70: Per <rdar://problem//7519048> K86/K87: change U7000 to 353S2929
Changed U7000 from 353S2392 to 353S2929
Updated APN text note

2010-01-08: 2.0.0
csa 45: Per <rdar://problem//7524364> K86/K87: change SATA HDD D2R passive EQ values
Removed NOSTUFF from C4585, C4586
Removed OMIT from R4585, R4586
Deleted BOM table that stuffed the bypass option
Changed R4585, R4586 to 114S0905 (27.4 ohm, 1%)
Changed C4585, C4586 to 151S4713 (47pF, 5%)

2010-01-13: 2.1.0
csa 4: Per <rdar://problem//7540383> K86: Update CPU part number to 337S3792
Changed U1000 CPU:1.2GHZ BOMPTION from 337S3779 to 337S3792

2010-01-13: 2.2.0
csa 4: Cosmetic: changed text sizes and alignment
Per <rdar://problem//7540522> K86/K87: Production Debug Components
Changed B85-1003 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG
Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG
Diff from the two changes above:
Toggled:
BMON:NRGN:YES ==> VREFMRGN:NO
BMON:ENG ==> BMON:PROD
BMON:PRG ==> BMON:PRG
SENS.R:ENG ==> SENS.R:PROD
Removed:
DEBUG_ADC, S0P000_ISL, EFI_DEBUG, MCPPLL_LDO, EXT1V05, MCP_T_DIODE_SENSOR, XDP_CONN
Unchanged:
LPCPLUS_DEVEL_BOM, SMC_DEBUG:YES, XDP
Added LPCPLUS_CON to K87_DEVEL_ENG (does not change BOM for DVT)
Changed all instances of K87_DEBUG:xxxx to K87_DEBUG:xxxx
Changed all instances of K87_DEVEL:xxxx to K87_DEVEL:xxxx
csa 51: (Per <rdar://problem//7540522> K86/K87: Production Debug Components)
Changed J5100 BOMPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT

2010-01-15: 2.3.0
csa 74: Per <rdar://7525313 > K86 CPU loadline, OCP update
Keeping K86 and K87 as identical for csa 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86.
IMVP6.1PHASE BOM Table:
R7417 changed to 7.87K (APN 114S0305)
R7416 added to BOM Table, 16.9K (APN 114S0336)
Added IMVP6.2PHASE BOM option to R7416 for K87's 13.7K
csa 74, csa 70: Per <rdar://7542674 > K86/K87 Text note change
Cleaned up text notes for 1phase, 2phase, and edp #s per radar request.

2010-01-18: 2.4.0
csa 4: Per <rdar://problem//7549122> K86/K87: Switch to new BOM group structure
Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes)
Changed BOM group structure to match that in the radar (see PDF attached to radar)
Net change was to move LPCPLUS to the 639 (from the 805)
Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD
Per <rdar://problem//7544528> K86/K87: Update MCP83 description
Changed description for 337S3876 to "IC:MCP83M-A02_31X31MM_BGA1368"
Per <rdar://problem//7544527> K86/K87: Fix schematic symbol for Q2355, Q2356
Started syncing with K6
syncing with K6 to pick up new symbols for Q2355 and Q2356
Should switch syncing back to T27 once it is updated there
csa 37: Per <rdar://problem//7548728> K86/K87 Ethernet series R's need to be 0 ohmed
Changed R3700-R3795 to 115S0004 (0-ohm, 0402) from 22-ohm

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2010-01-19: 2.5.0
csa 37: Per <rdar://problem//7554342> K86/K87: Change L3720 to 152S1182
Changed L3720 to 152S1182 (1N0,Pwr,SHD,4.7uH,20%,0.91A,31X31X12MM) for lower ESR

2010-01-22: 2.6.0
csa 4: Per <rdar://problem//7571706> K86/K87: Add E3T EEE code for K86 to schematic
Added root to EEE table for E3T
Changed BOMPTIONS to be mutually exclusive (changed "_" to ":")

2010-01-28: 2.7.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
- pg. 62: changed R6211 to 22 0Hms
- pg. 67: no stuffed R6712 and R6713
csa 45: Per <rdar://problem//7561961> K87 EMC: Radiated Emissions: Right Audio emissions fail
Added L4530, L4531 (APN 155S0137) to SIL connector pins
csa 97: Per <rdar://problem//7589365> K86/K87: Compensation settings change to provide more phase margin, reduce ripple
Changed C9729 from 22nF to 10nF (114S0315) and removed NOSTUFF
Changed C9705 from 8.2nF to 33nF (132S0131)
Changed C9706 from 120pF to 220pF (131S2225)

2010-02-02: 2.8.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
- pg. 67: added BOM options for U6780, R6712, and R6713 to support MAX14560 and MAX14504
csa 97: Changed R9710 from 7.32K 0402 to 7.68K (APN 114S0304) to support old K84 panel
csa 4: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON

2010-02-15: 2.9.0
2010-02-15: 2.10.0
csa 54: Broke sync with T27. Per <rdar://problem//7605797> K69/K86/K87 sensor IN1C unreliable
U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF

2010-02-16: 2.11.0
Resync with T27 and K6. Clean up and rerelease schematic.

2010-02-18: 2.12.0
Per <rdar://7644836> K87 power component update
csa 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF
csa 75: R7572 changed to 147K
csa 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF
Per <rdar://7634730> K86/K87: add an RC on the LVDS_IG_BKL_PWM
csa 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKL_PWM

2010-02-18: 2.13.0
Per <rdar://7670934> K86/K87: Hall eff documentation change. Substitute 607-6831 for doc purposes
csa 69: J6955 BOMPTION change to OMIT. Added BOM table with 607-6831 for J6955
Per <rdar://7488543> K86/K86 Task: Measure each Power supply in MLB
csa 74: For K86 only: C7434 = 0.1uF added, R7417 changed to 8.25Kohm
csa 12: For K86 only: C1272 = 330uF added.
Per <rdar://7695202> K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue
csa 97: U9700 changed to APN 353S2965

2010-02-18: 2.17.0
Per <rdar://7695179> K86/K87 schematic: Change audio jack part number for new connector cap
csa 67: J6700 changed from APN 514-0718 to 514-0750

2010-02-25: 2.18.0
Per <rdar://7695811> K86/K87 schematic: add additional 639 for differentiation between Foxconn and Molex DIMM connectors
csa 4: MOLEX_DDR_CONN added to Module Parts, removed from Alternate table. Added second 639 and EEEE # to BOM table

2010-02-25: 2.19.0
Per <rdar://7670515> K87:EMC:ESD: System hangs on air/contact discharge to MPM connector
csa 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added

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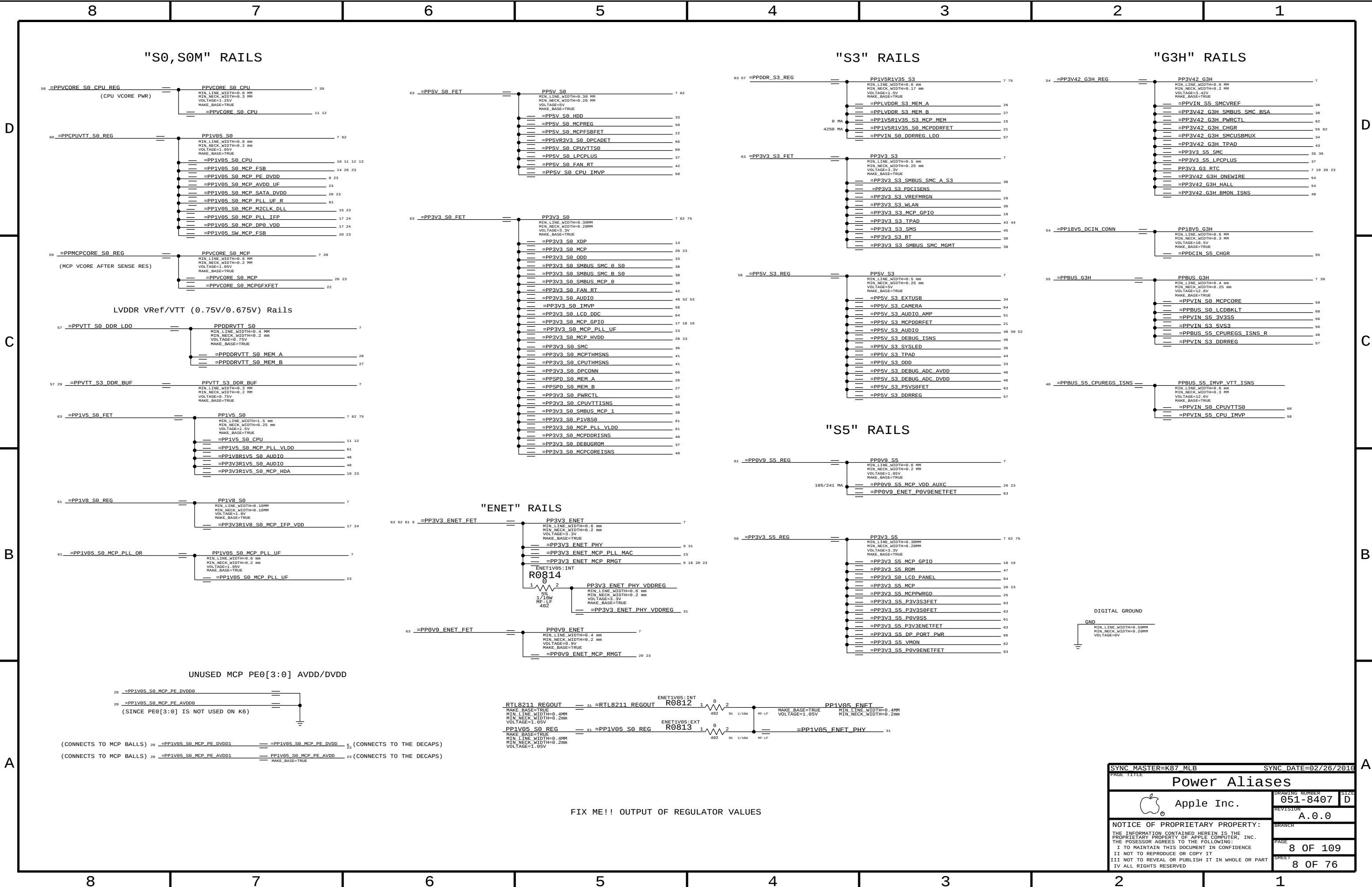
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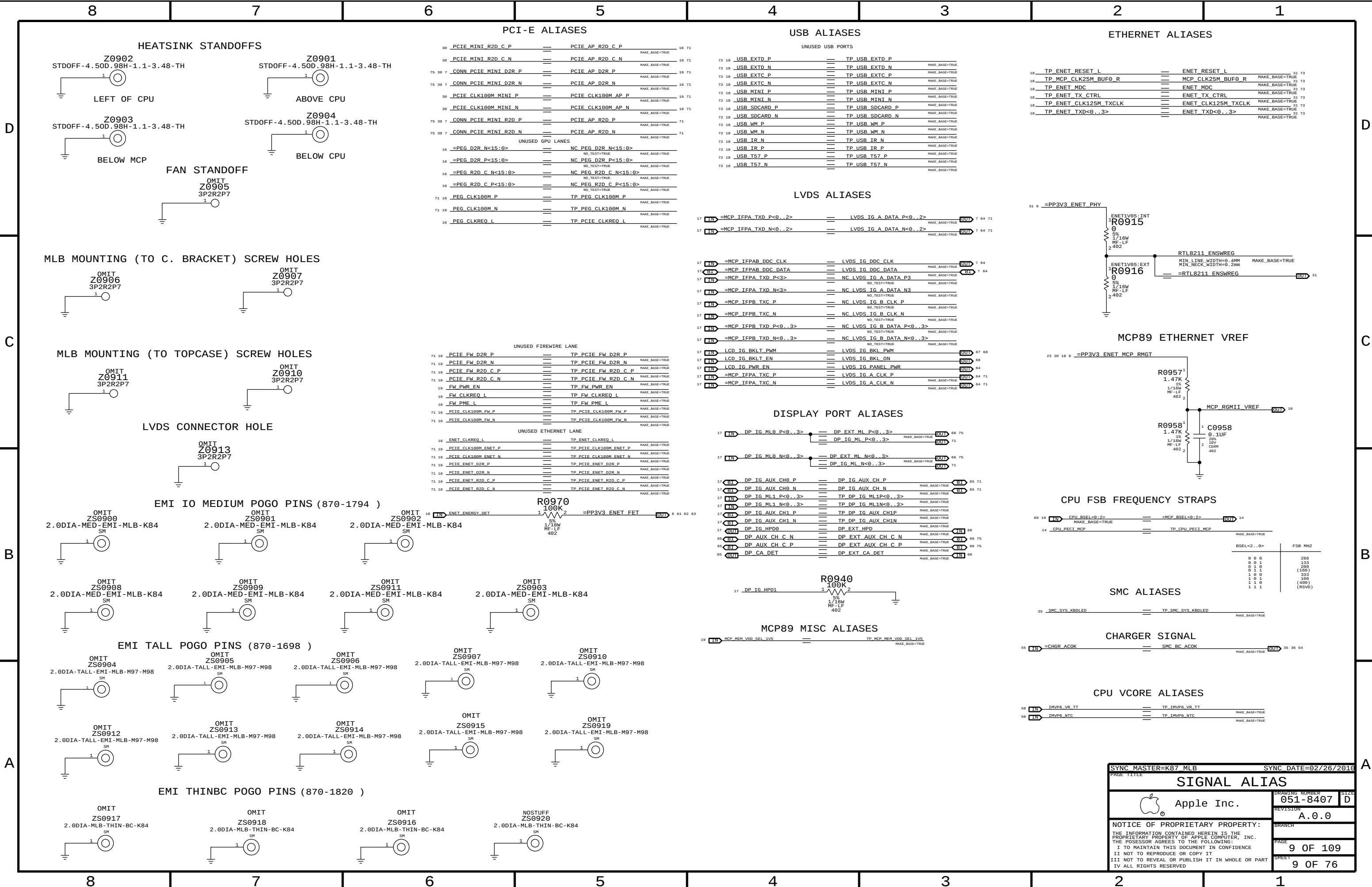
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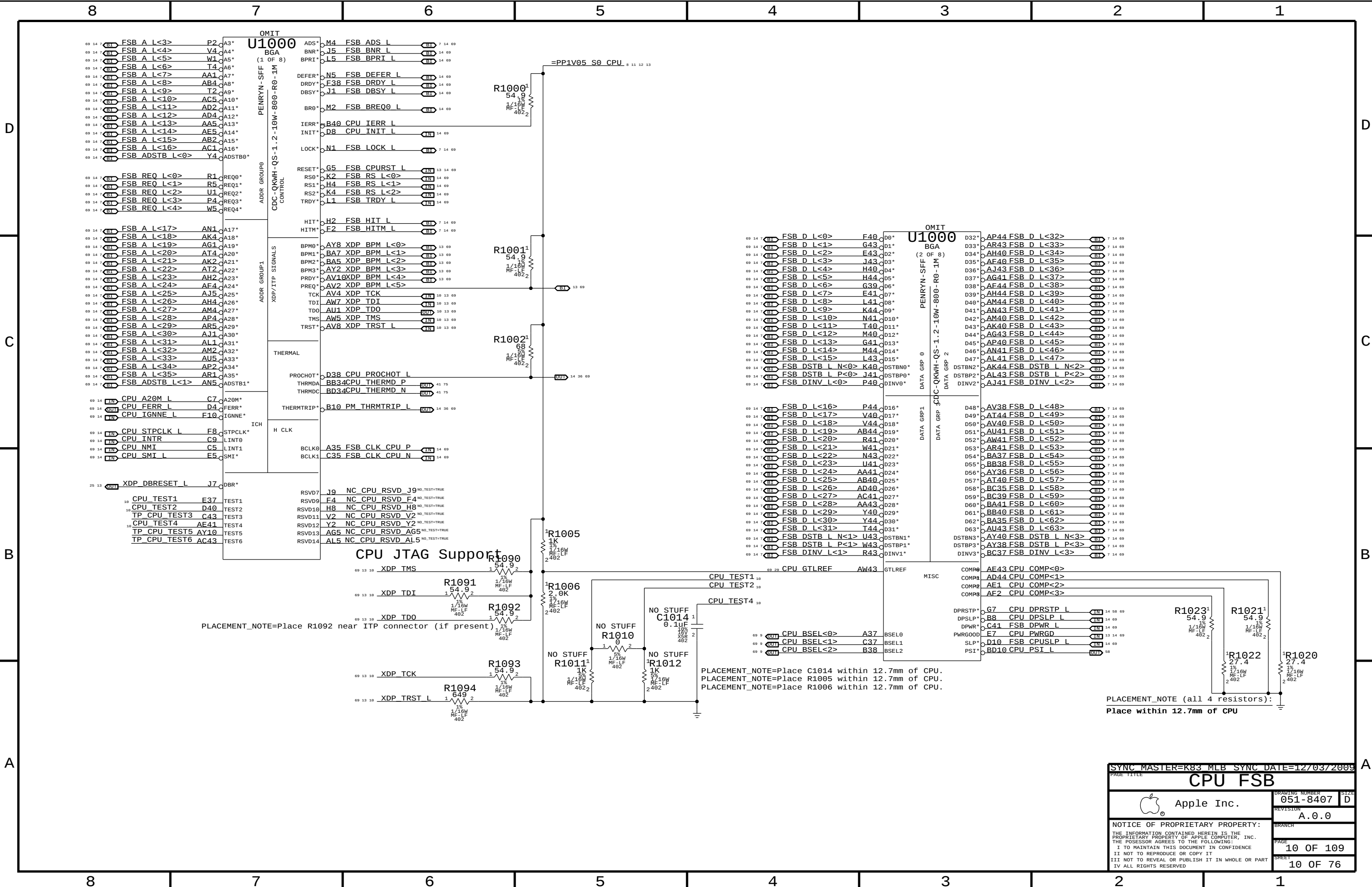
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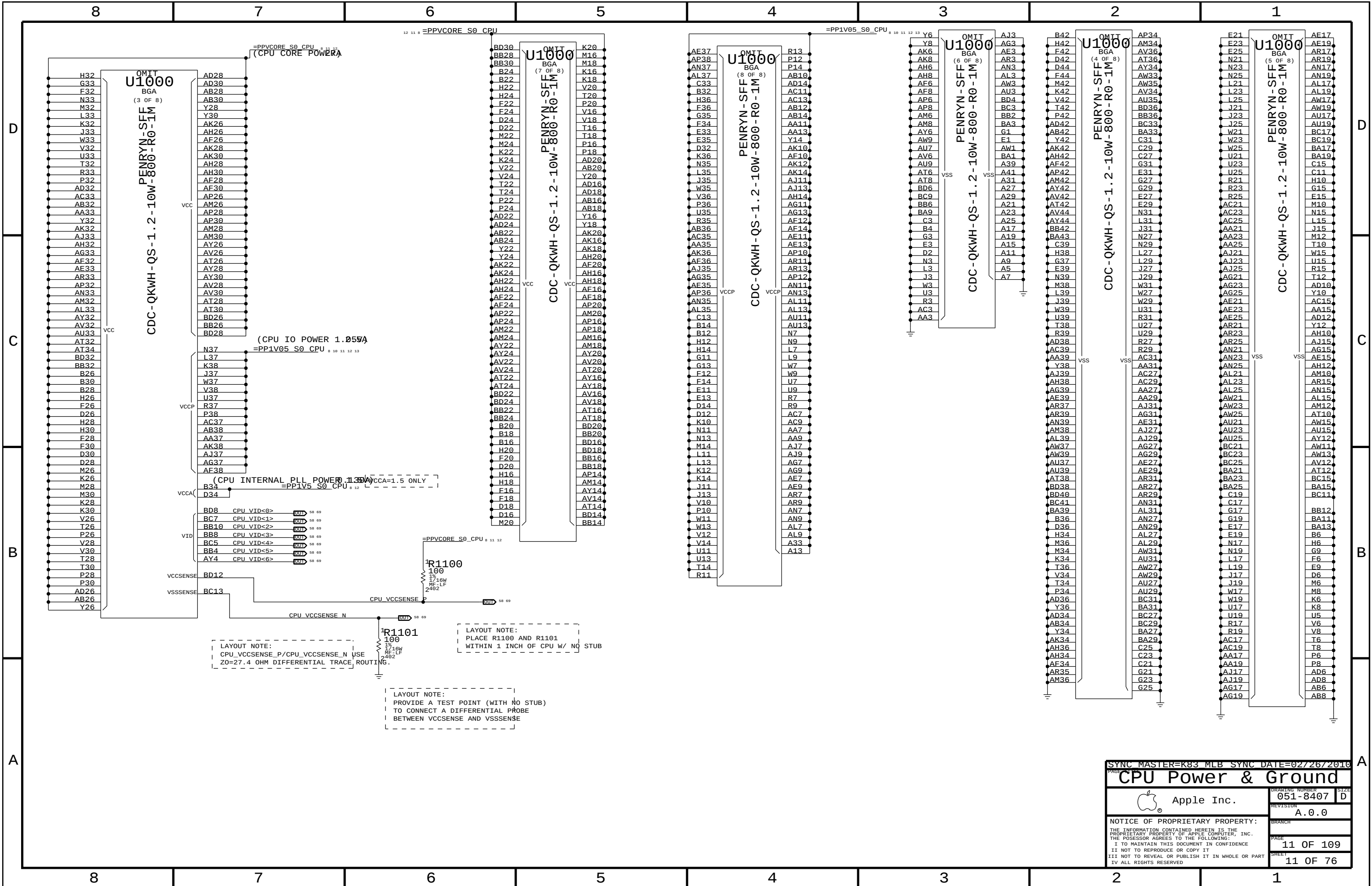


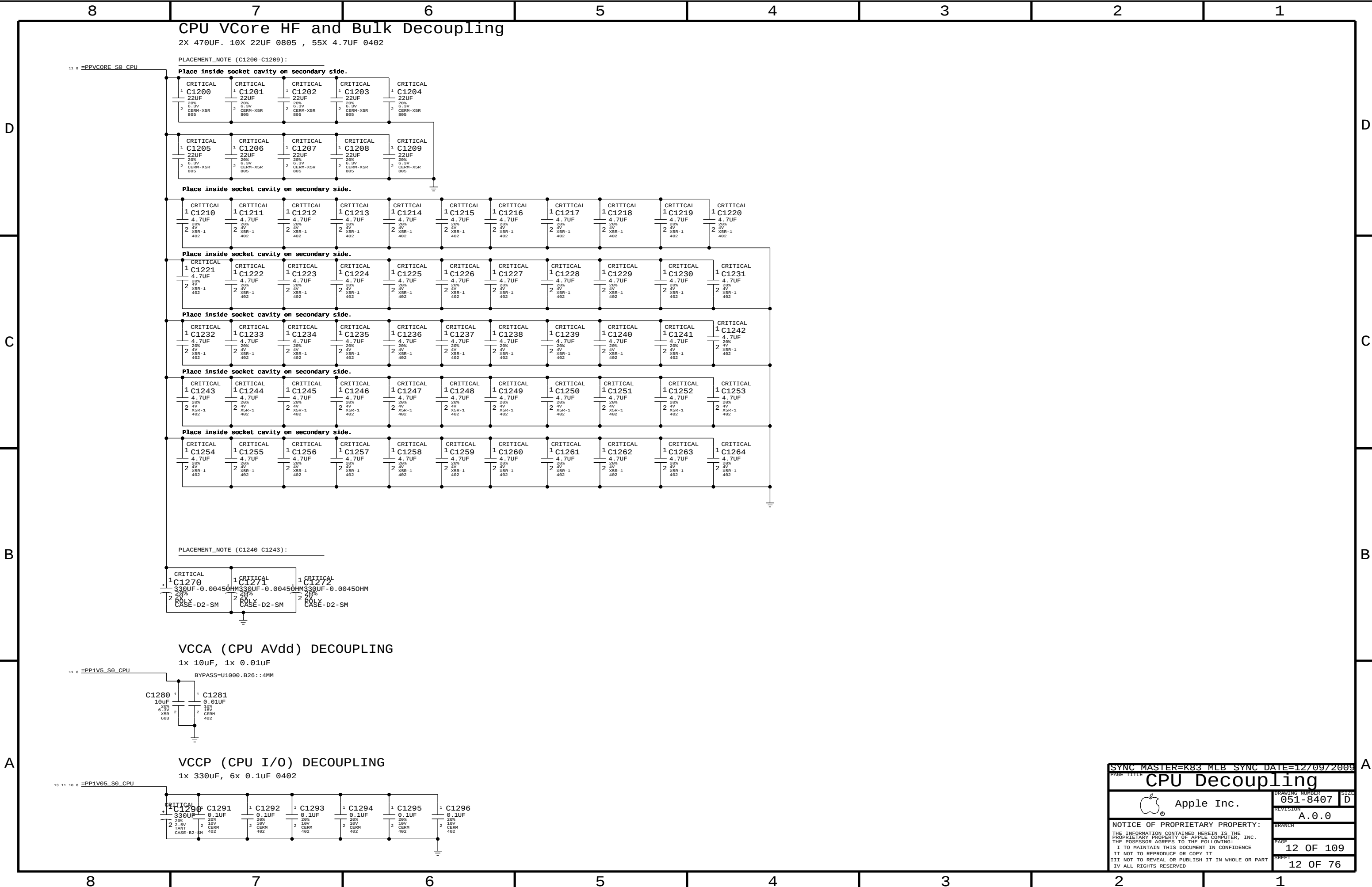
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CPU Decoupling

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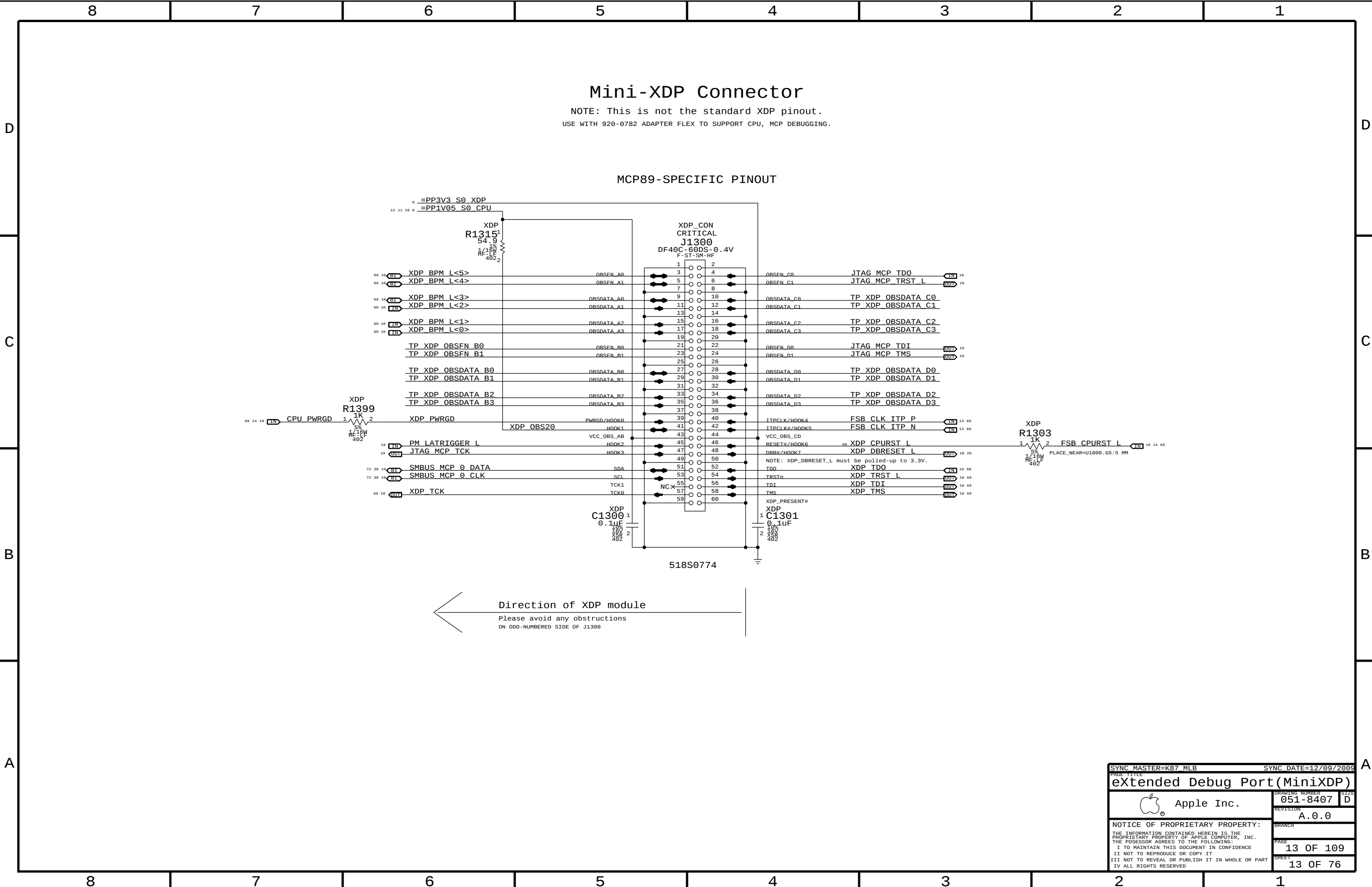
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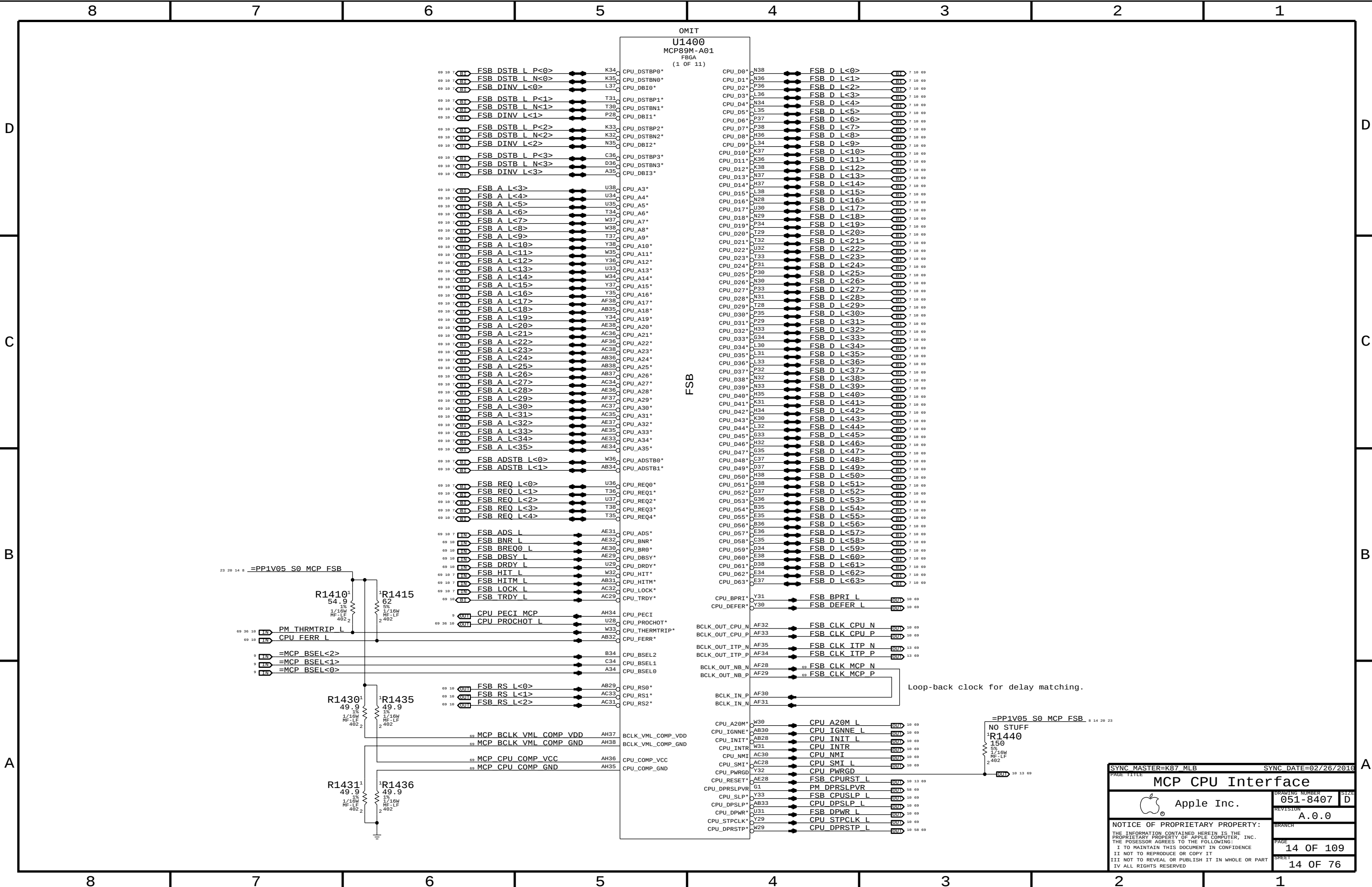
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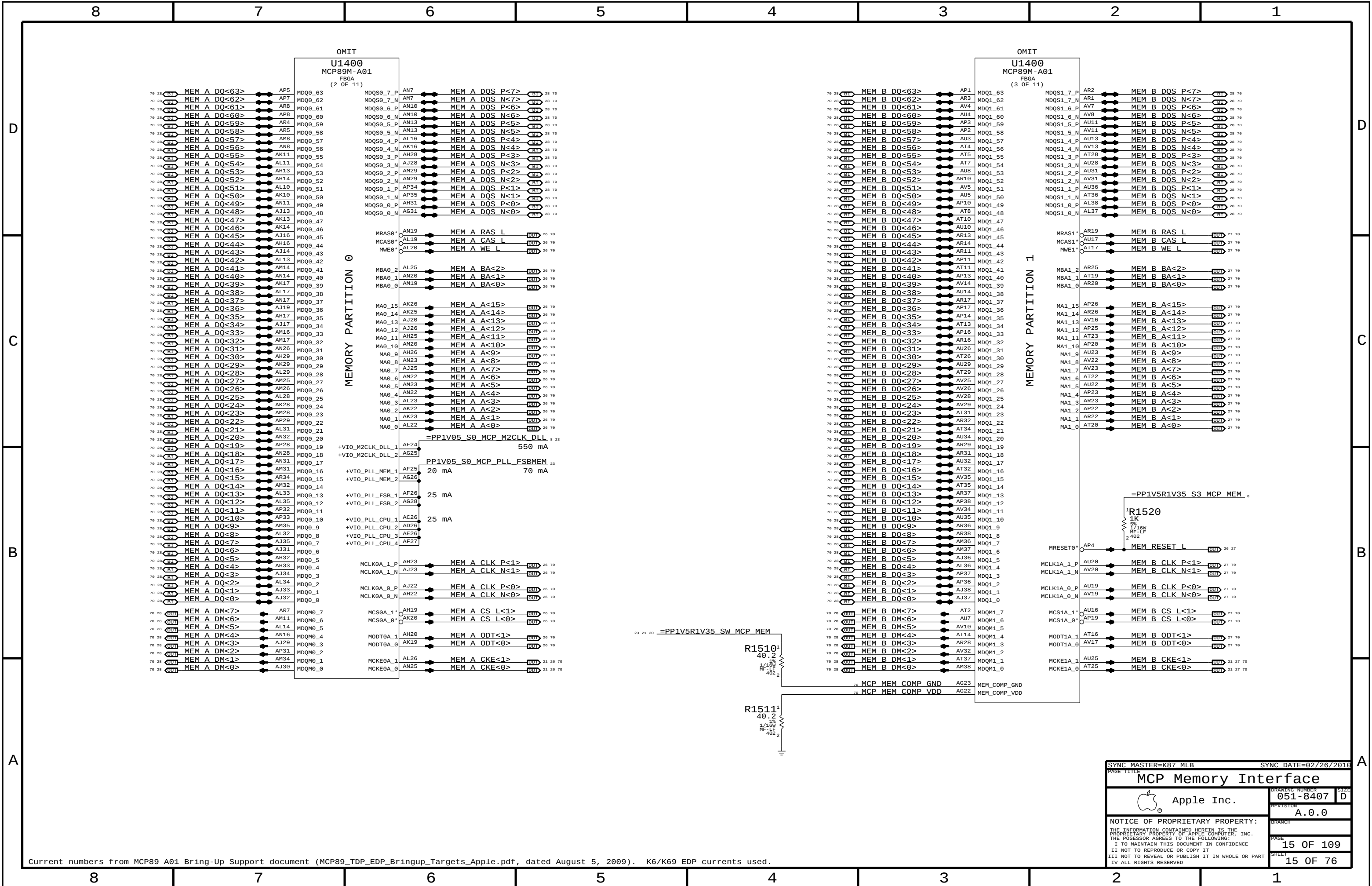
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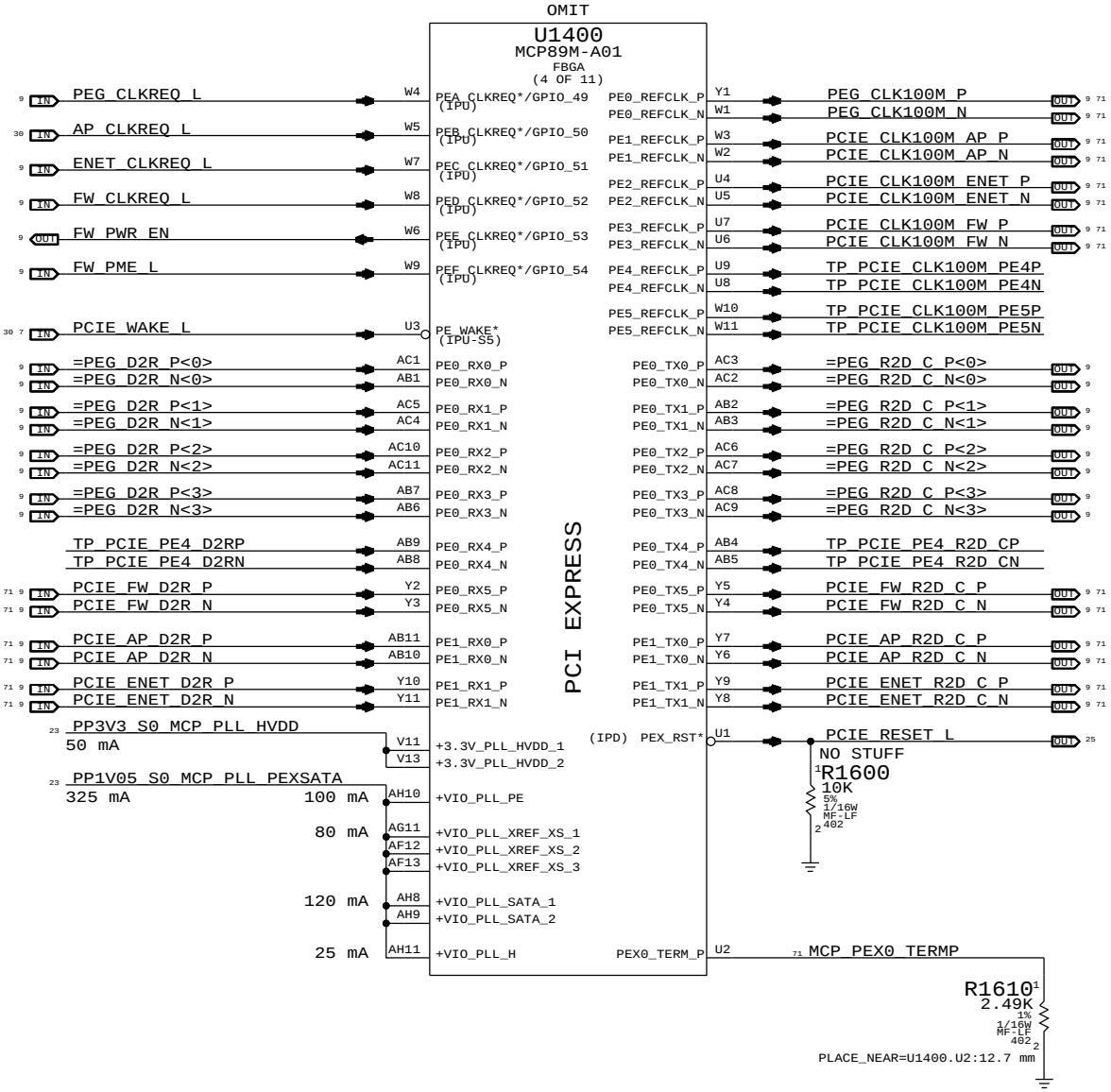
A

D

C

B

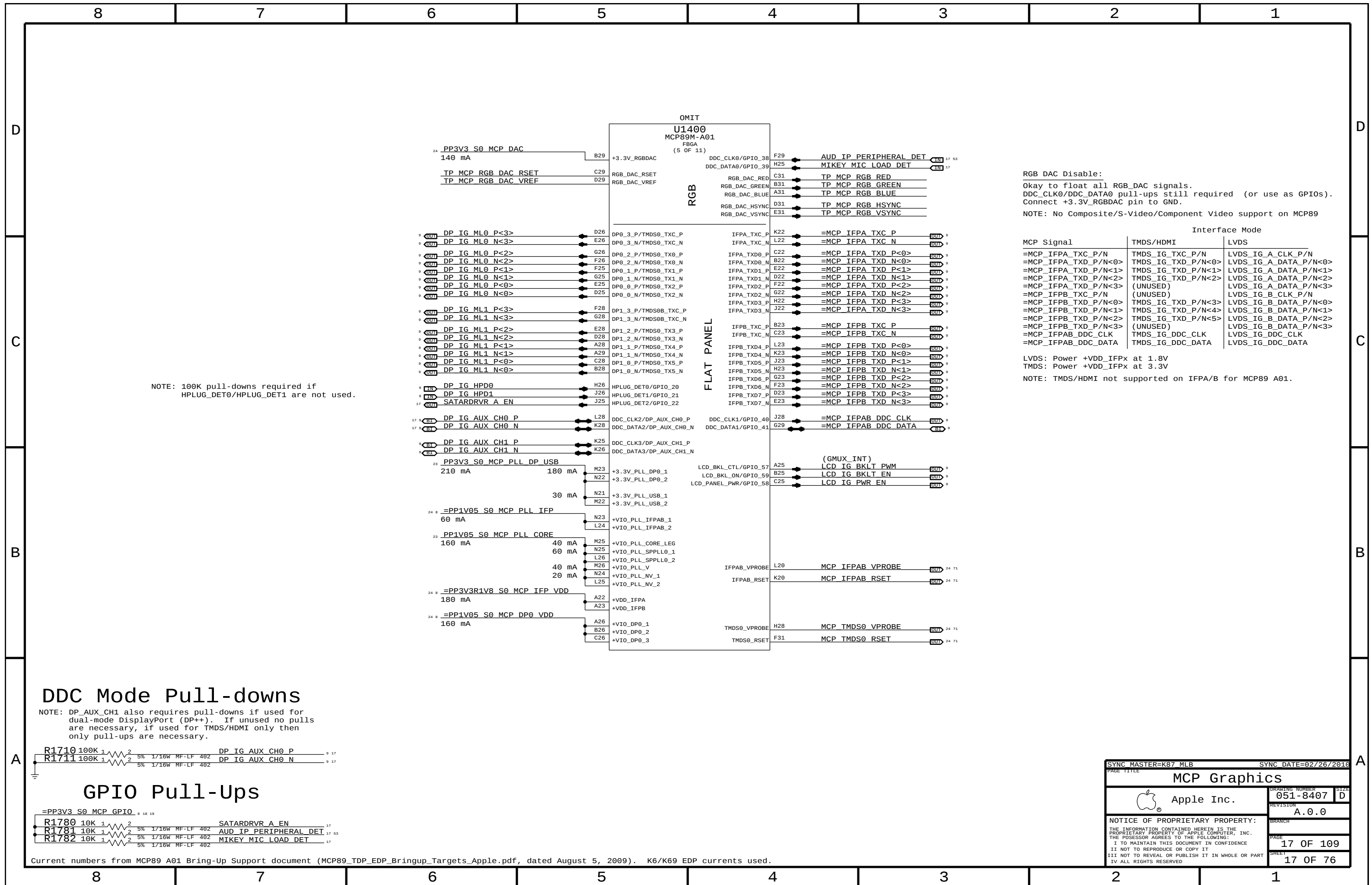
A

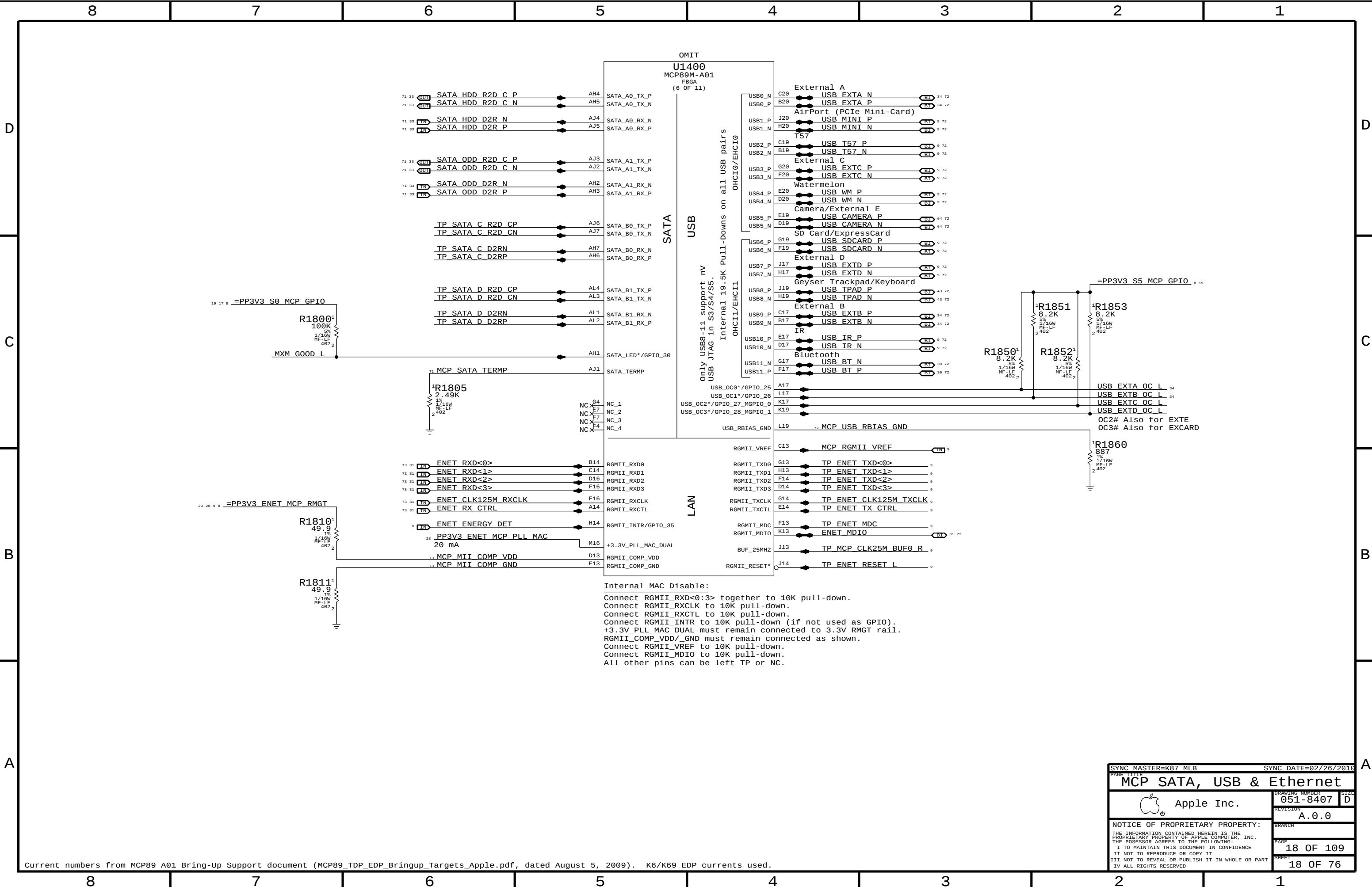


PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND





Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K87 MLB

SYNC DATE=02/26/2016

MCP SATA, USB & Ethernet

Apple Inc.

051-8407

A.0.0

18 OF 109

18 OF 76

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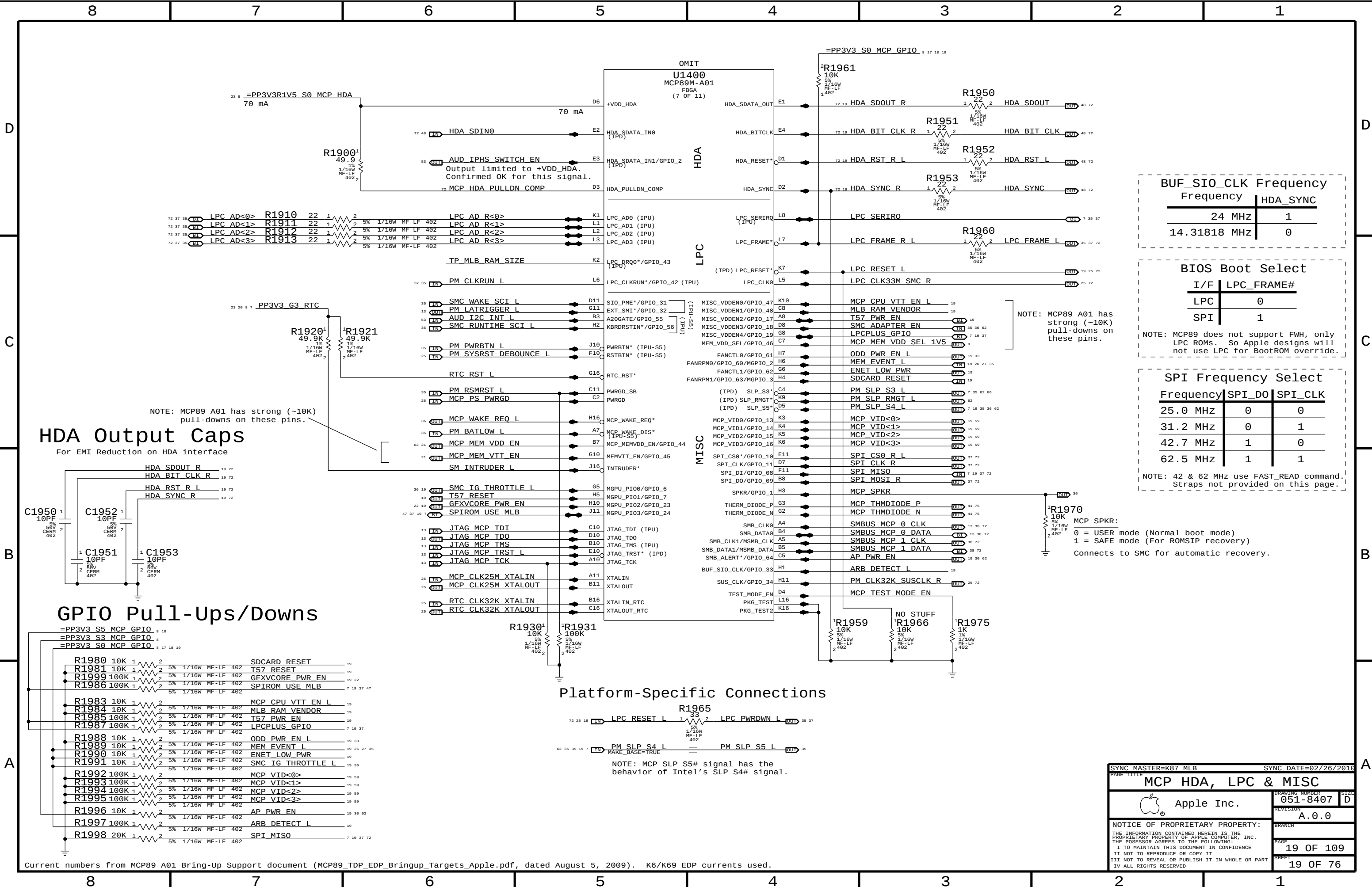
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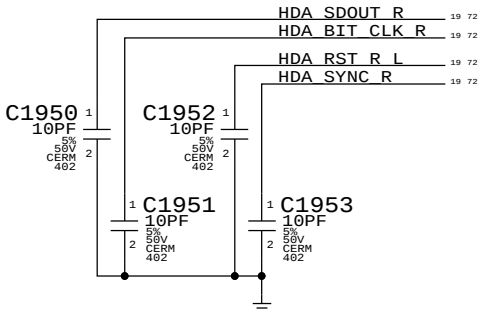
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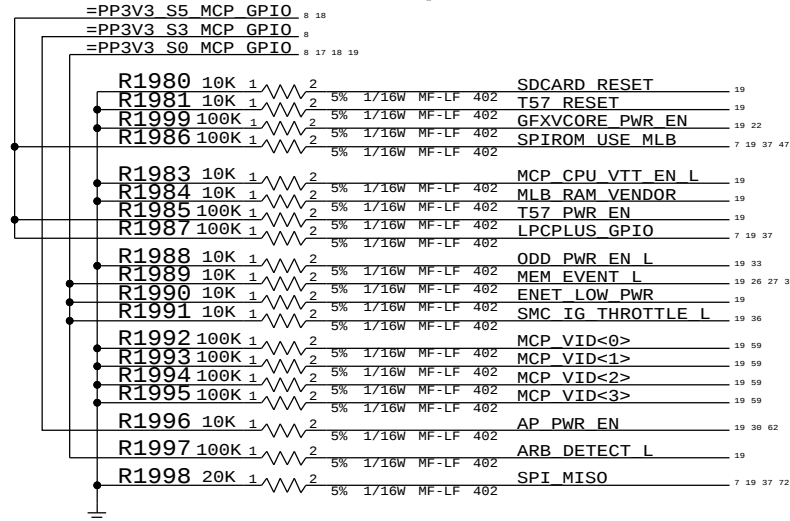


HDA Output Caps

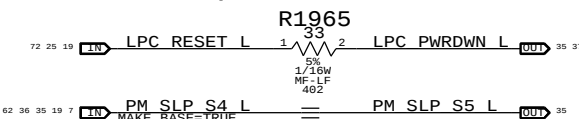
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal.

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

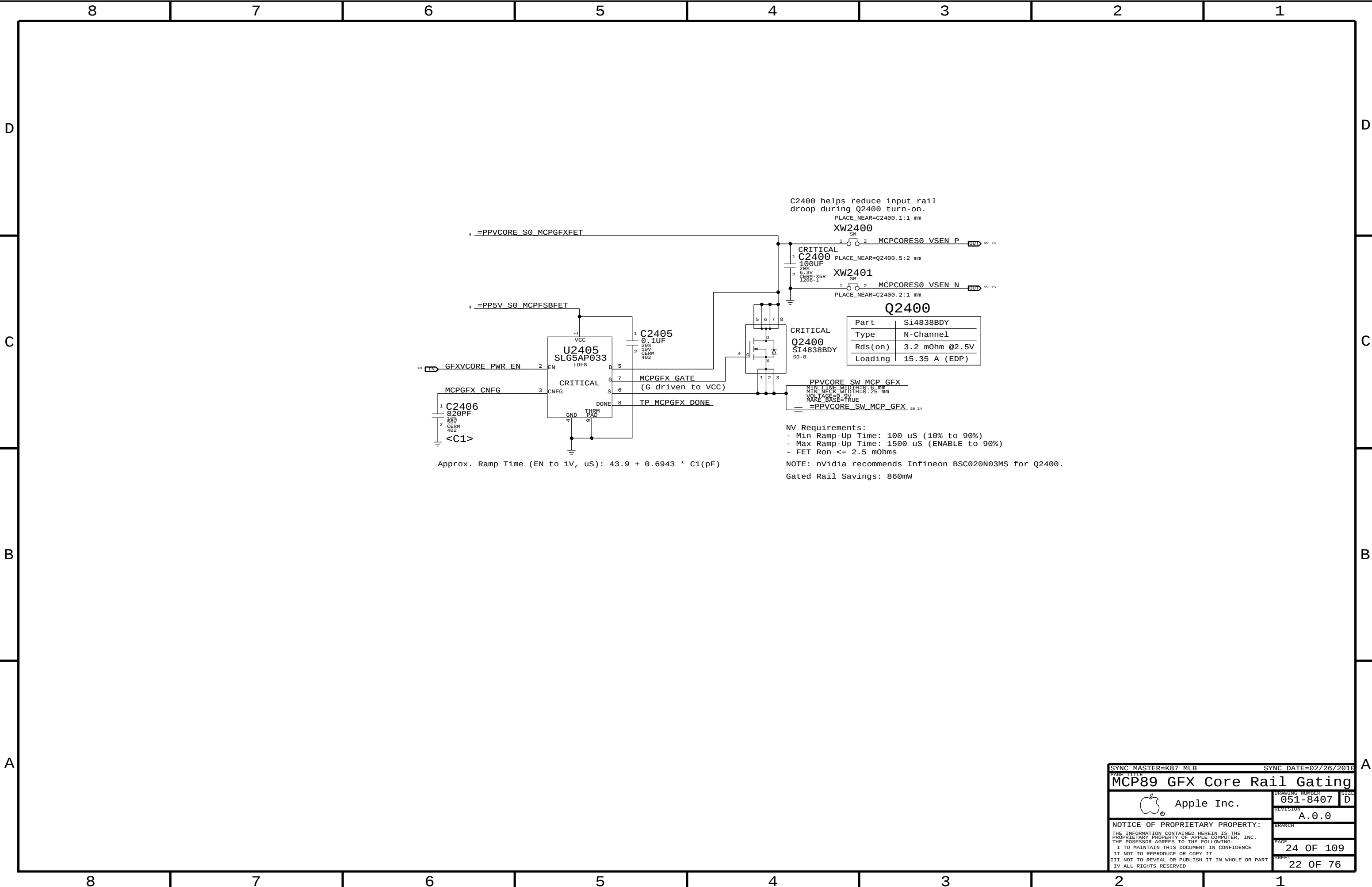
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

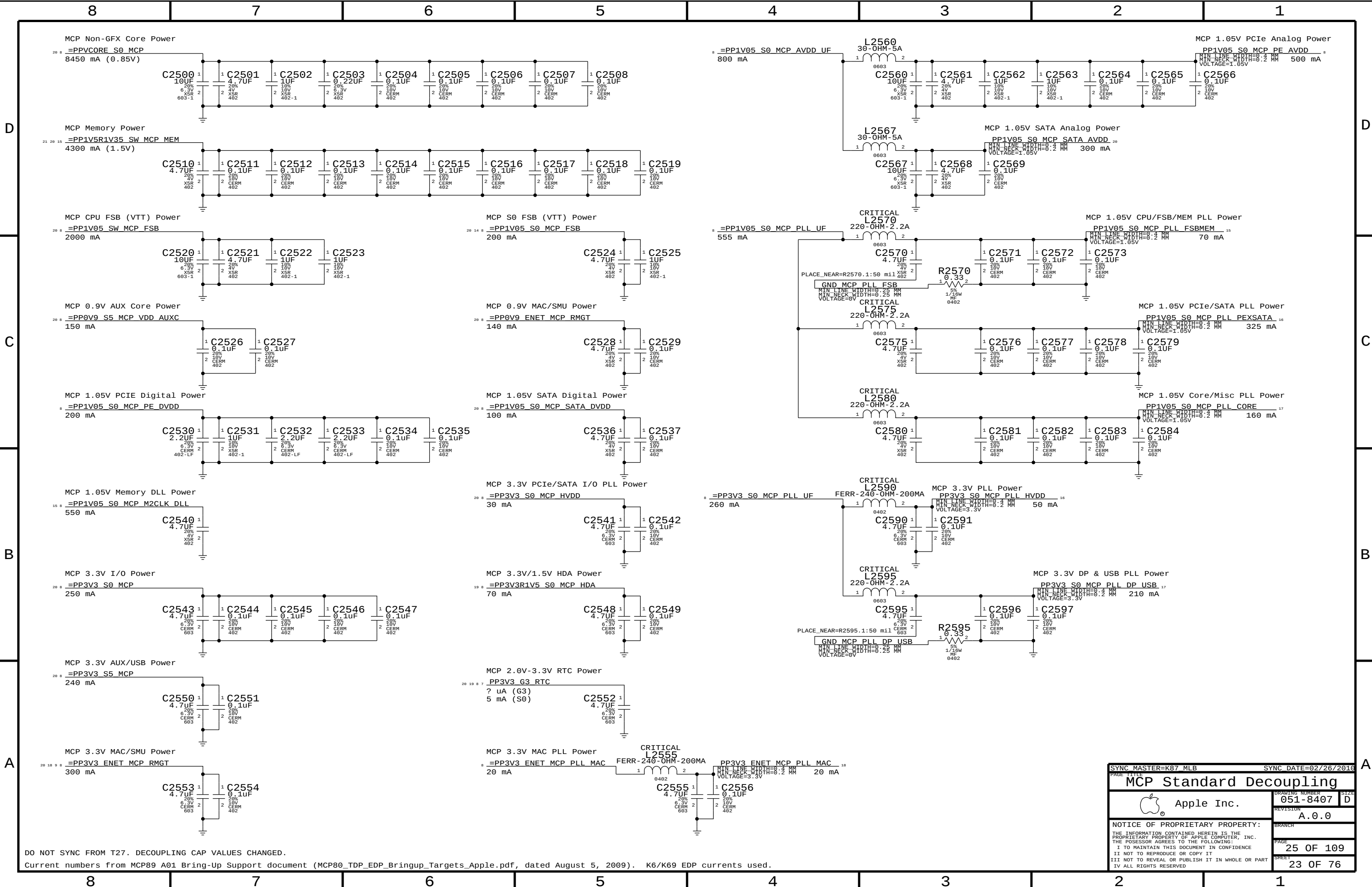
NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

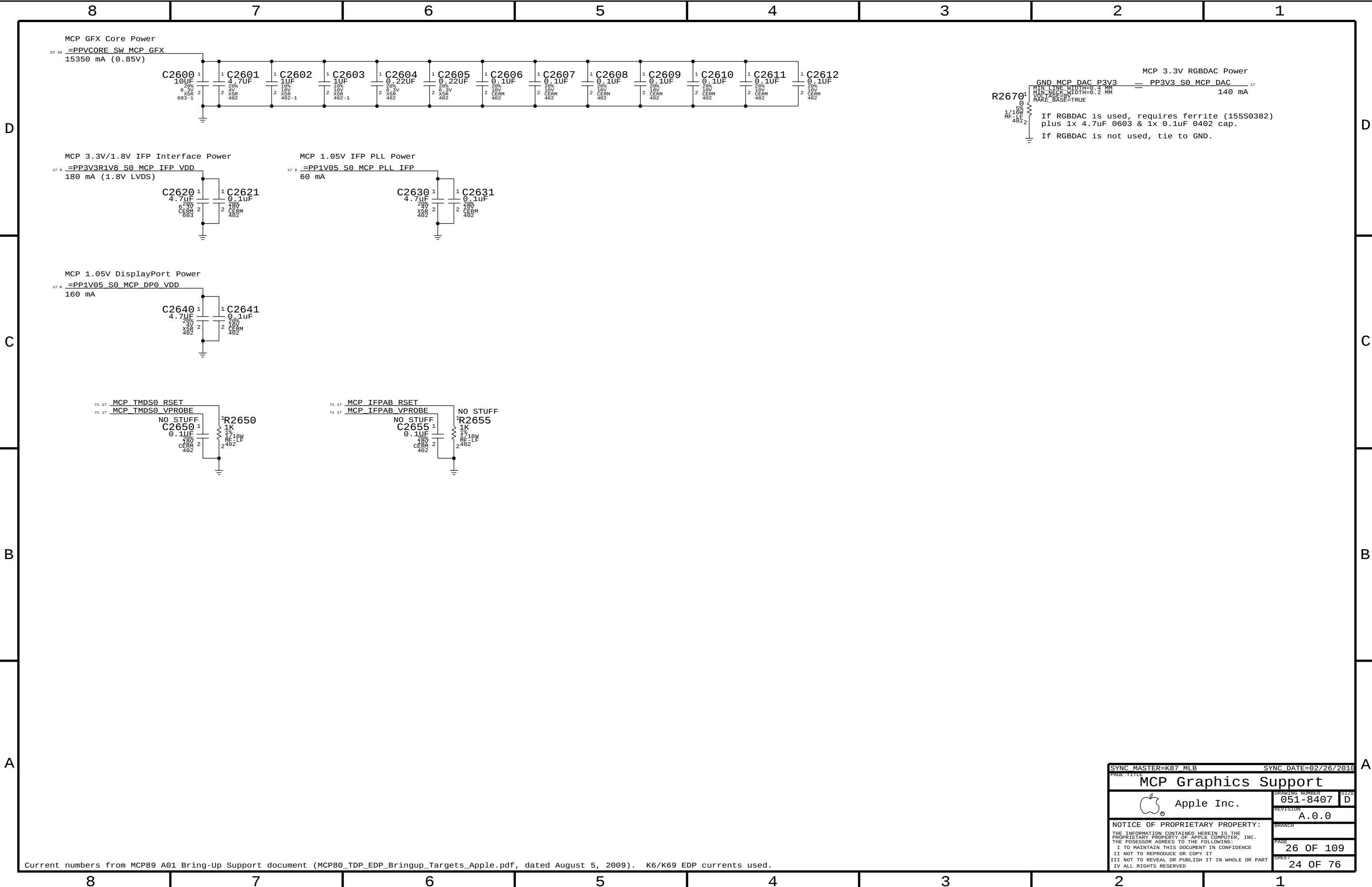
SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016			
PAGE TITLE					
MCP HDA, LPC & MISC					
Apple Inc.		DRAWING NUMBER	051-8407		
		REVISION	A.0.0		
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		PAGE	19 OF 109		
		SHEET	19 OF 76		





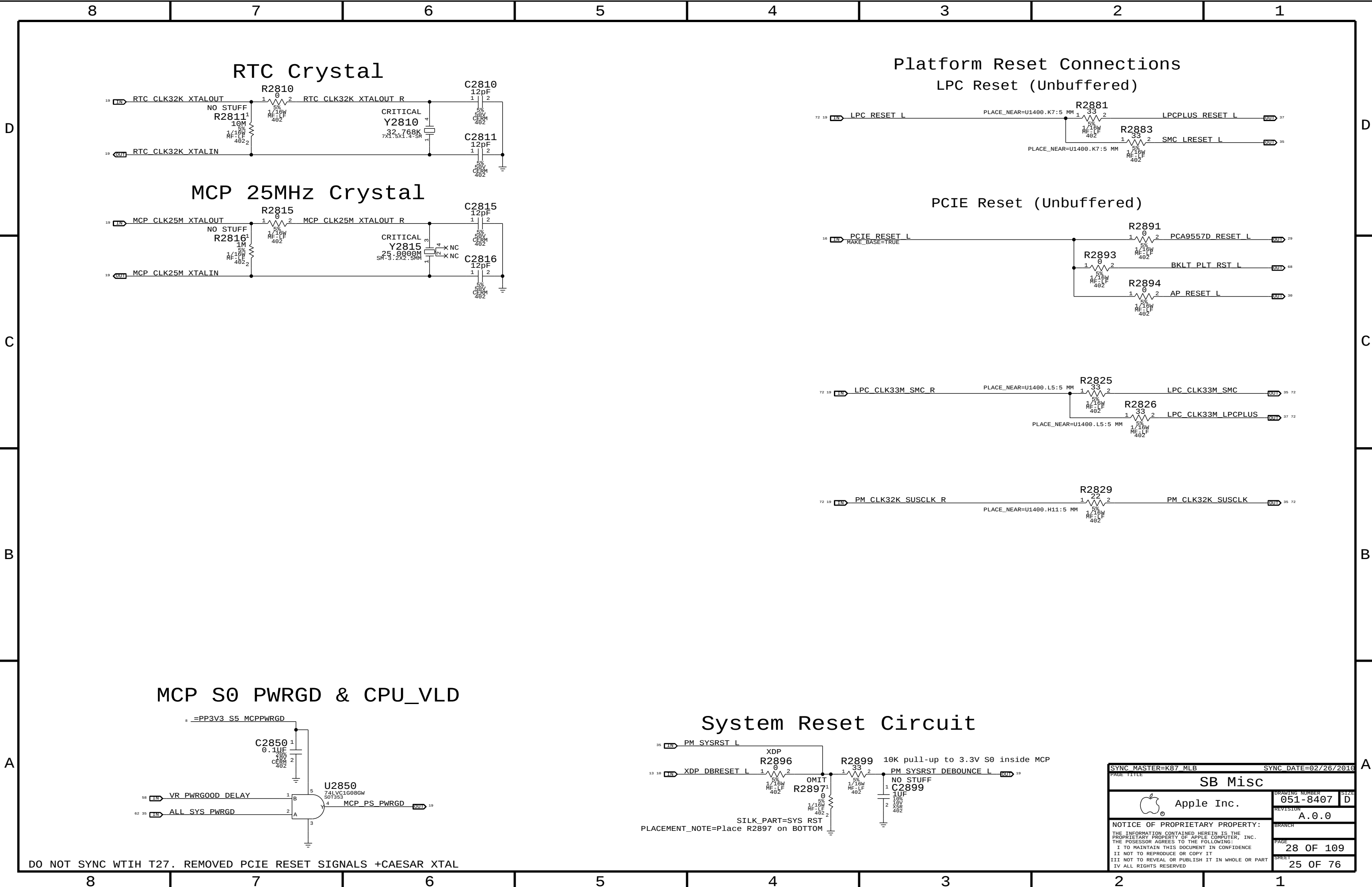
DO NOT SYNC FROM T27. DECOUPLING CAP VALUES CHANGED.
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE		MCP Standard Decoupling	
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		REVISION	A.0.0
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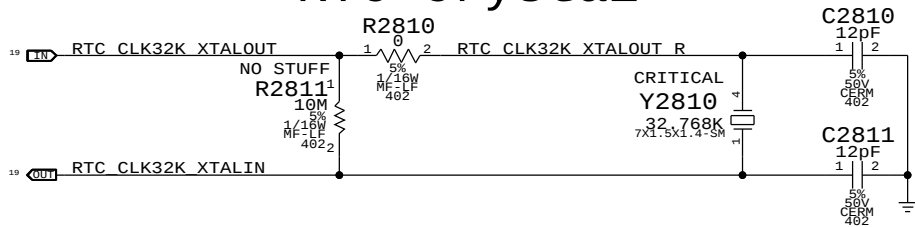


Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

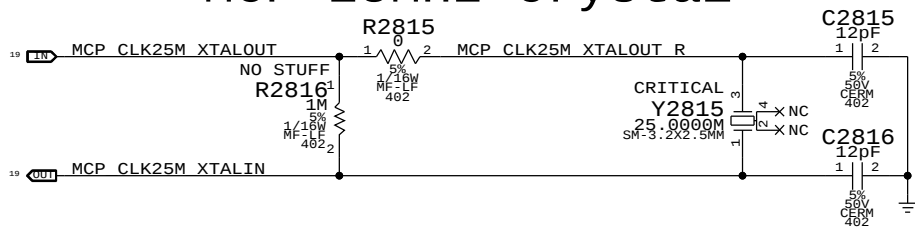
SYNC MASTER=K87 MLB		SYNC DATE=02/26/2010	
PAGE TITLE			
MCP Graphics Support			
 Apple Inc.		DRAWING NUMBER	051-8407
		REVISION	A.0.0
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		PAGE	26 OF 109
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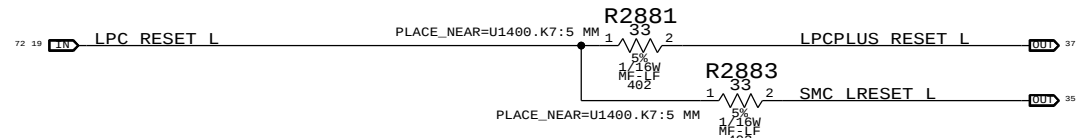
RTC Crystal



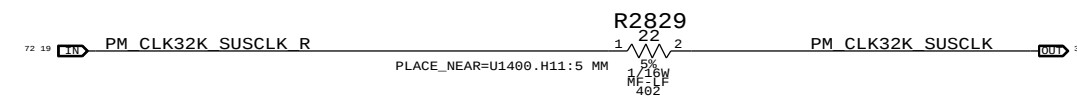
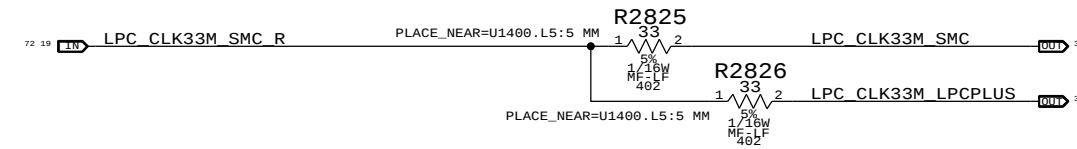
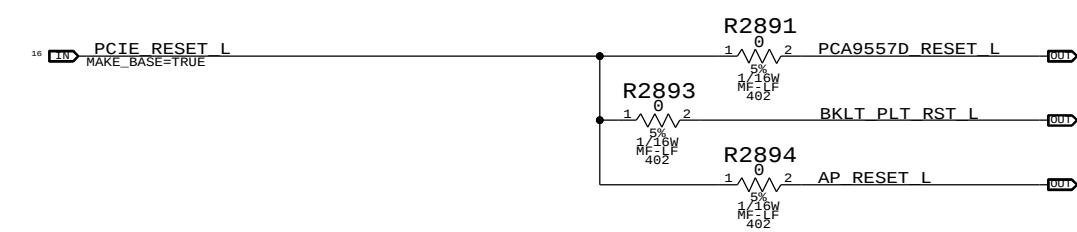
MCP 25MHz Crystal



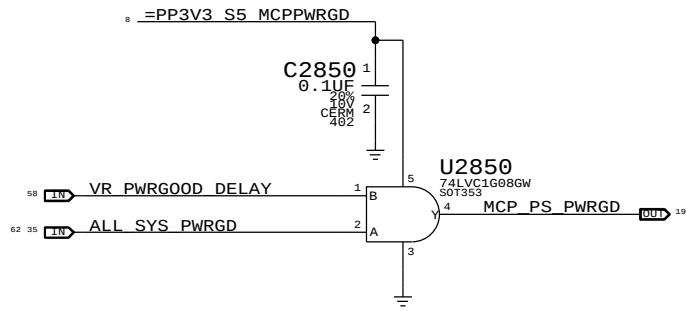
Platform Reset Connections
LPC Reset (Unbuffered)



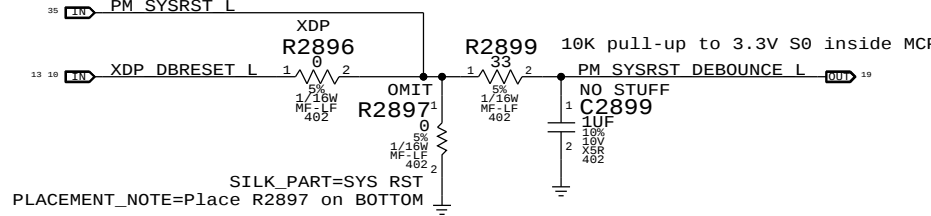
PCIE Reset (Unbuffered)



MCP S0 PWRGD & CPU_VLD



System Reset Circuit



PAGE TITLE		DRAWING NUMBER		SIZE	
SB Misc		051-8407		D	
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DO NOT SYNC WITH T27. REMOVED PCIE RESET SIGNALS +CAESAR XTAL

Page Notes

Power aliases required by this page:

- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

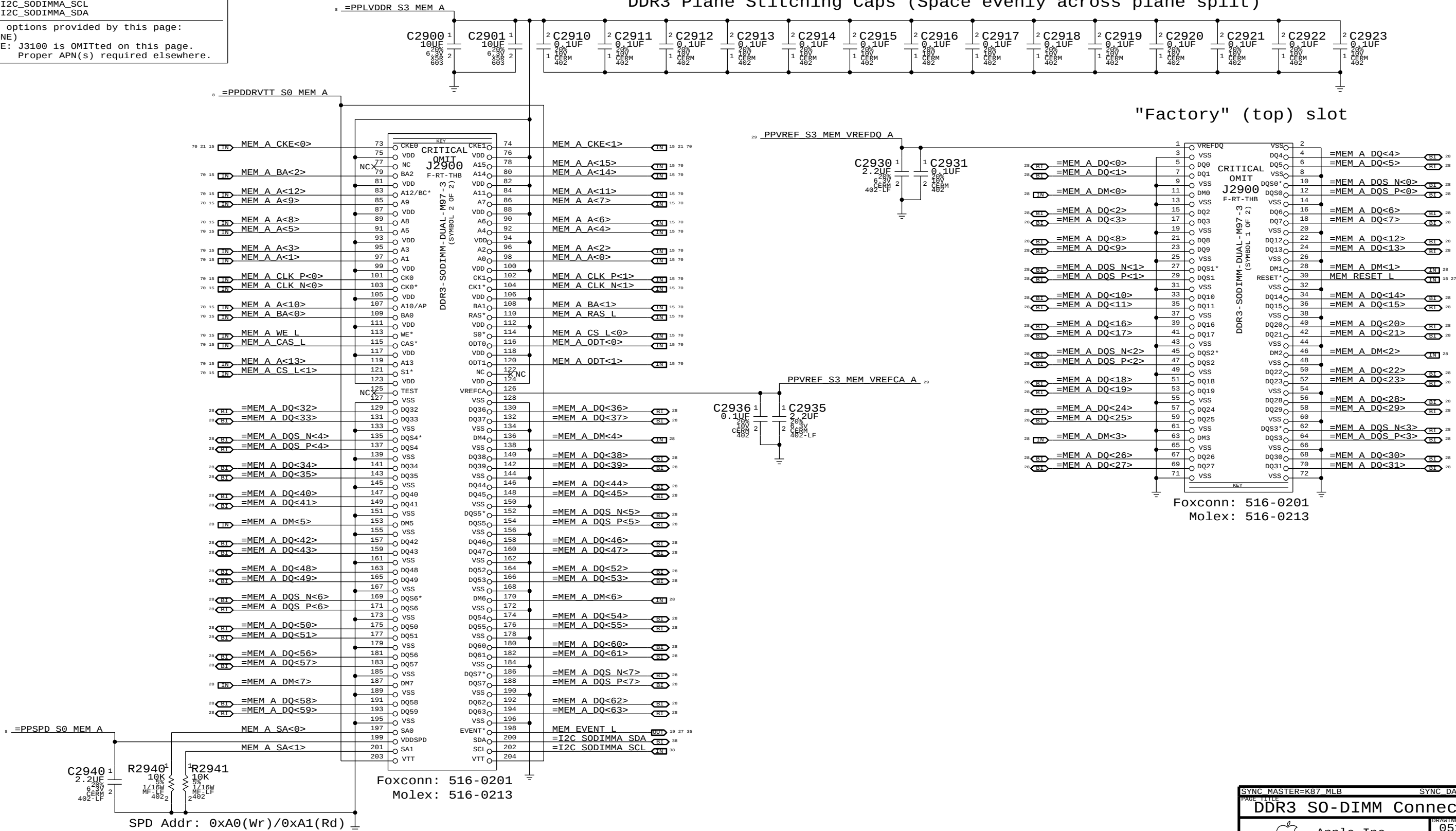
BOM options provided by this page:

(NONE)

NOTE: J3100 is OMITted on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

"Factory" (top) slot



SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
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Page Notes

Power aliases required by this page:

- =PPLVDDR_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

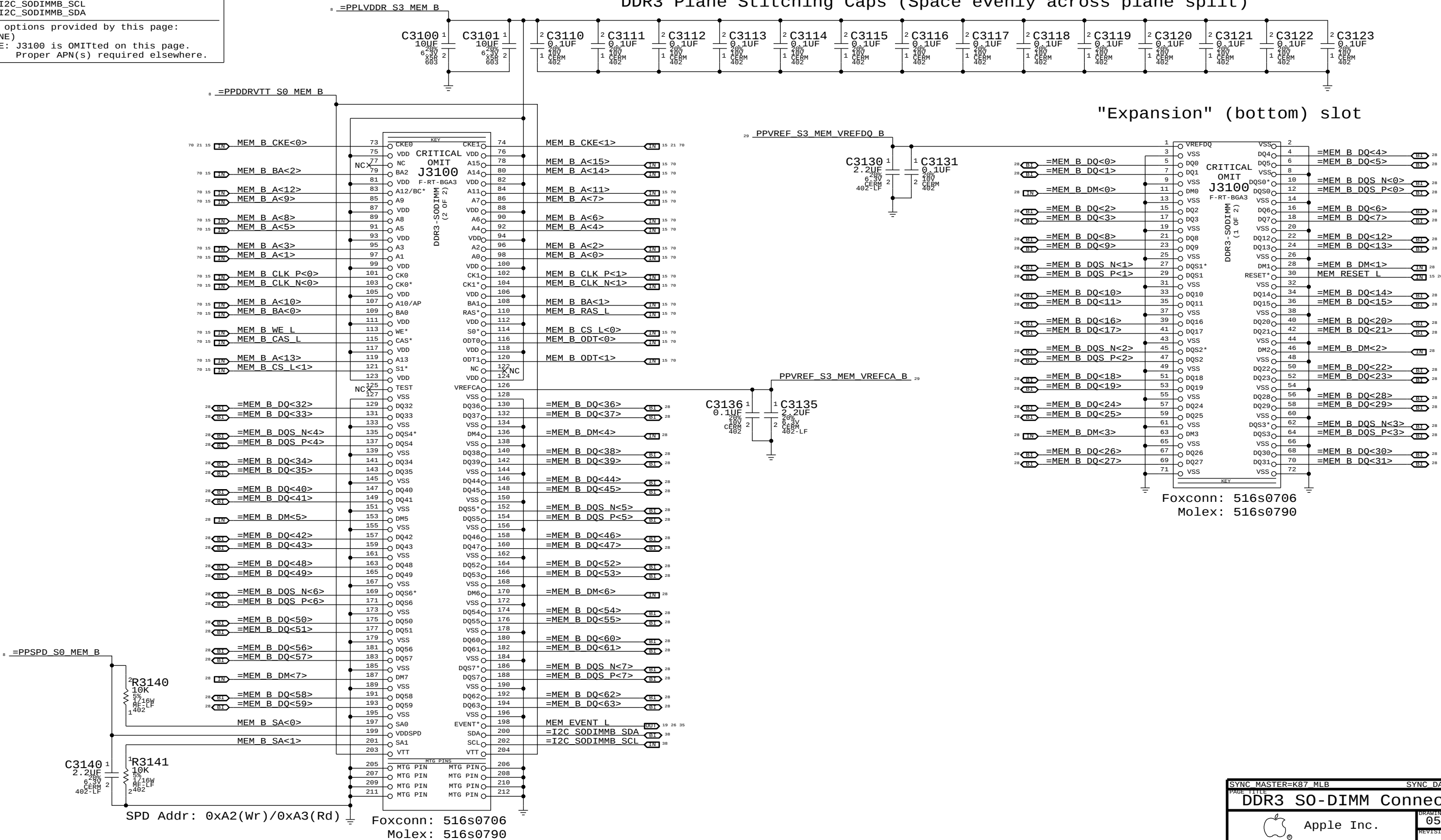
(NONE)

NOTE: J3100 is OMITted on this page.

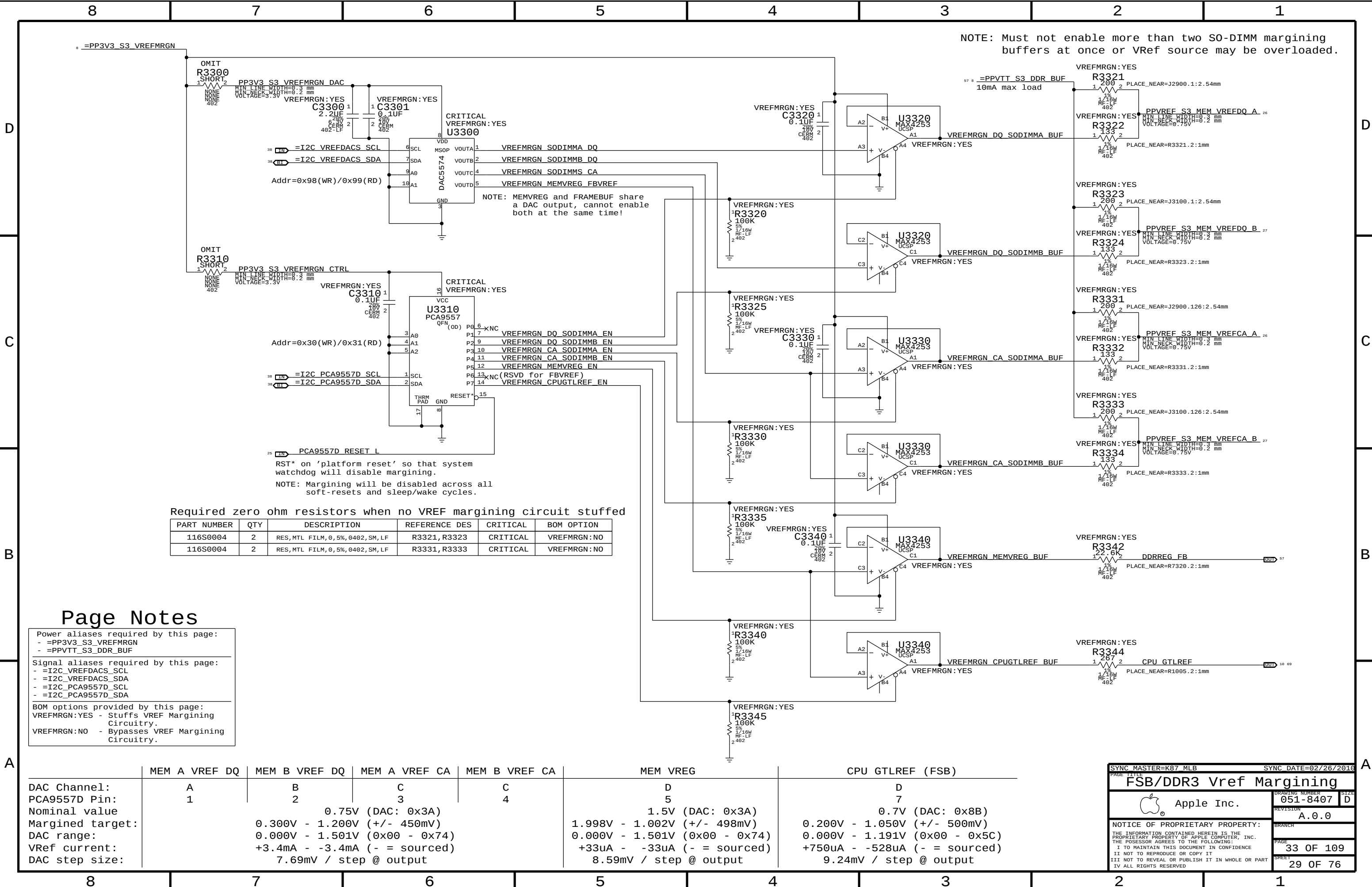
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

"Expansion" (bottom) slot



PAGE TITLE		SYNC DATE=02/26/2016	
DDR3 S0-DIMM Connector B		DRAWING NUMBER	
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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

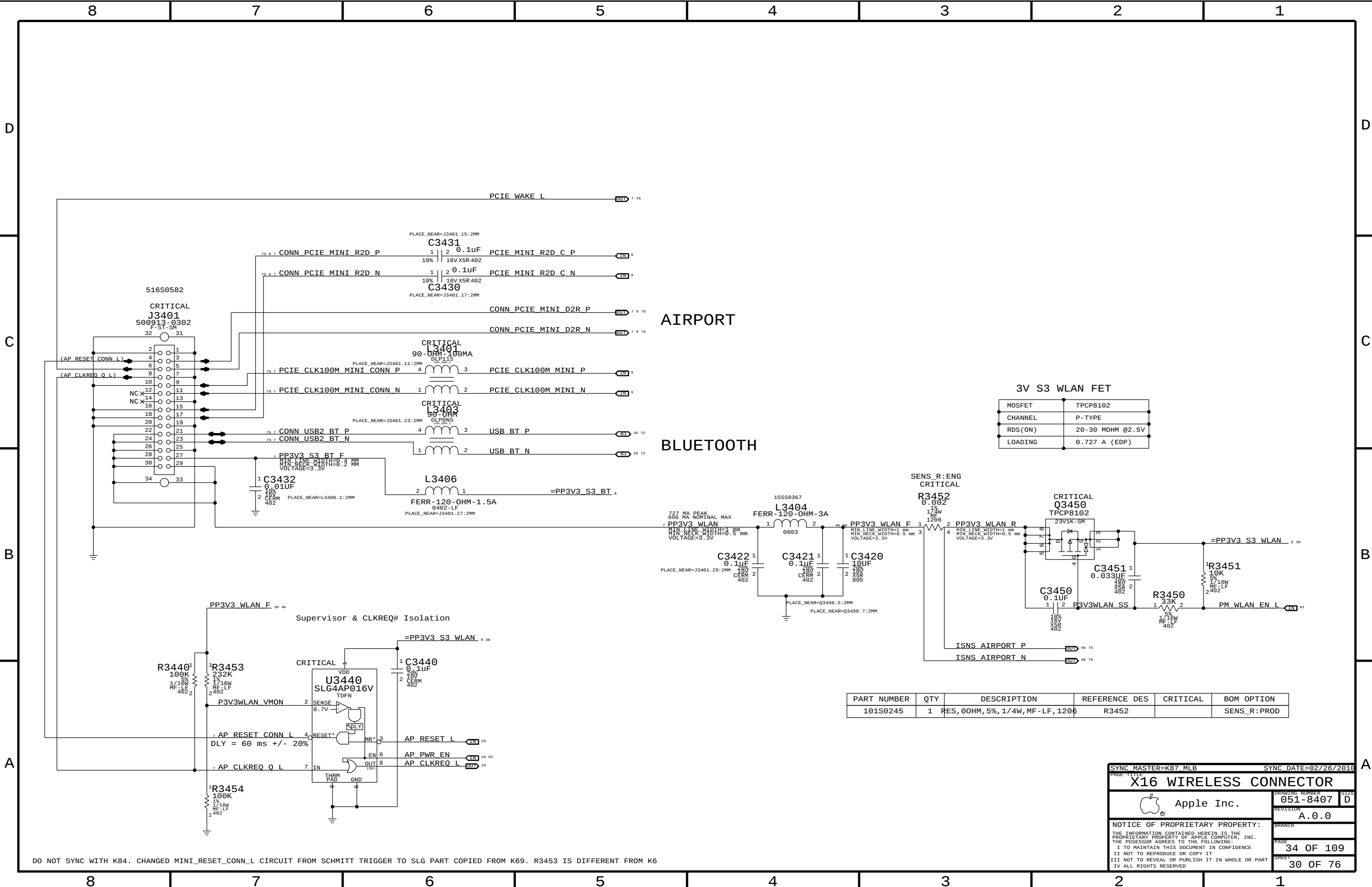
- VREFMRGN:YES - Stuffs VREF Margining Circuitry.
- VREFMRGN:NO - Bypasses VREF Margining Circuitry.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3321, R3323	CRITICAL	VREFMRGN:NO
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3331, R3333	CRITICAL	VREFMRGN:NO

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
FSB/DDR3 Vref Margining			
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		REVISION	A.0.0
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AIRPORT

BLUETOOTH

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	1	RES, 00HM, 5%, 1/4W, MF-LF, 1206	R3452		SENS_R:PROD

SYNC MASTER=K87 MLB

SYNC DATE=02/26/2016

X16 WIRELESS CONNECTOR

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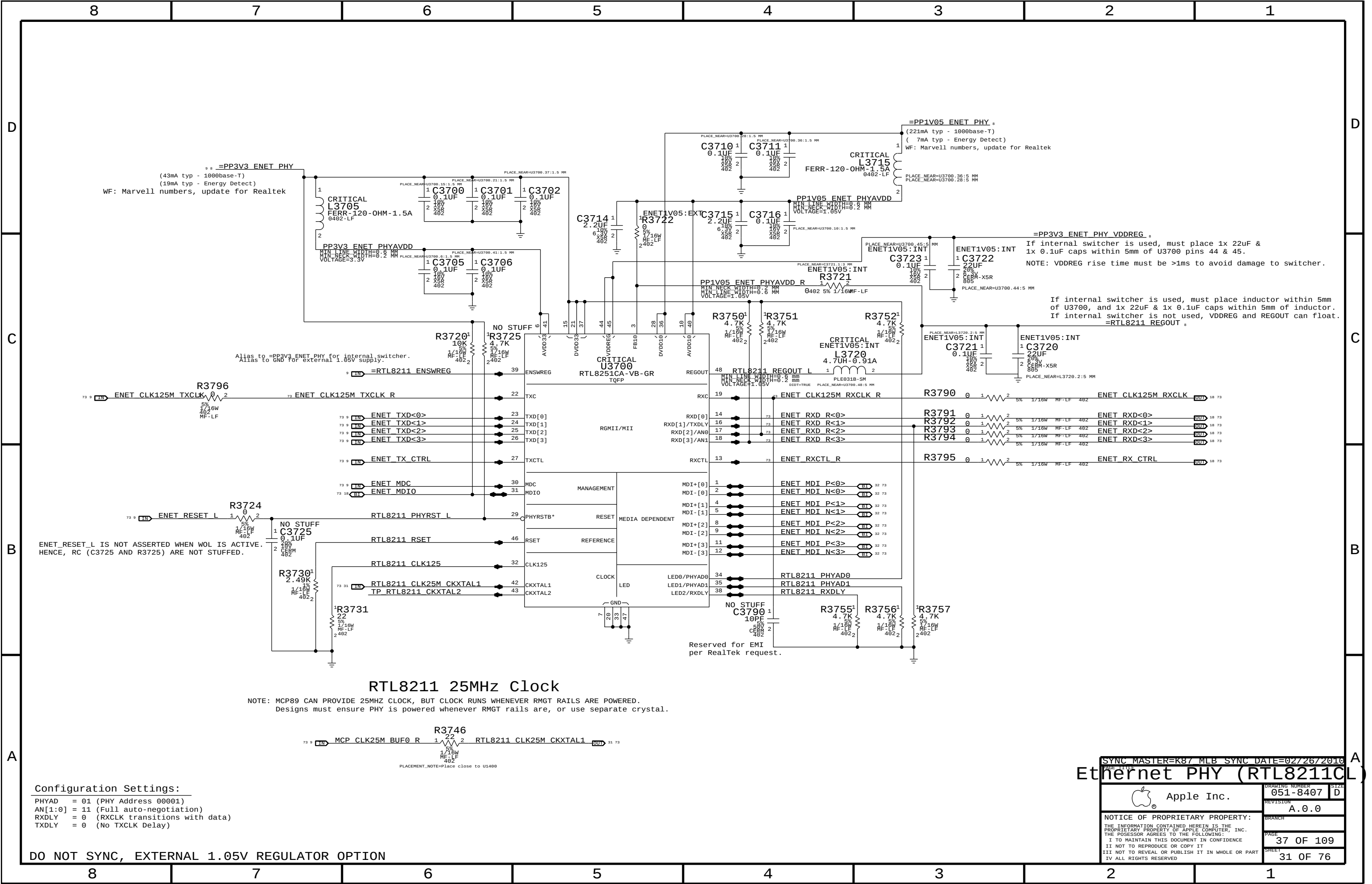
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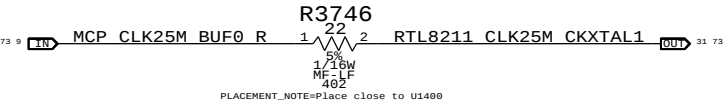
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DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6



RTL8211 25MHz Clock

NOTE: MCP89 CAN PROVIDE 25MHZ CLOCK, BUT CLOCK RUNS WHENEVER RMGT RAILS ARE POWERED.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



- Configuration Settings:
- PHYAD = 01 (PHY Address 00001)
 - AN[1:0] = 11 (Full auto-negotiation)
 - RXDLY = 0 (RXCLK transitions with data)
 - TXDLY = 0 (No TXCLK Delay)

DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION

SYNC MASTER=K87 MLB SYNC DATE=02/26/2010

Ethernet PHY (RTL8211C)

Apple Inc.

051-8407 D

REVISION A.0.0

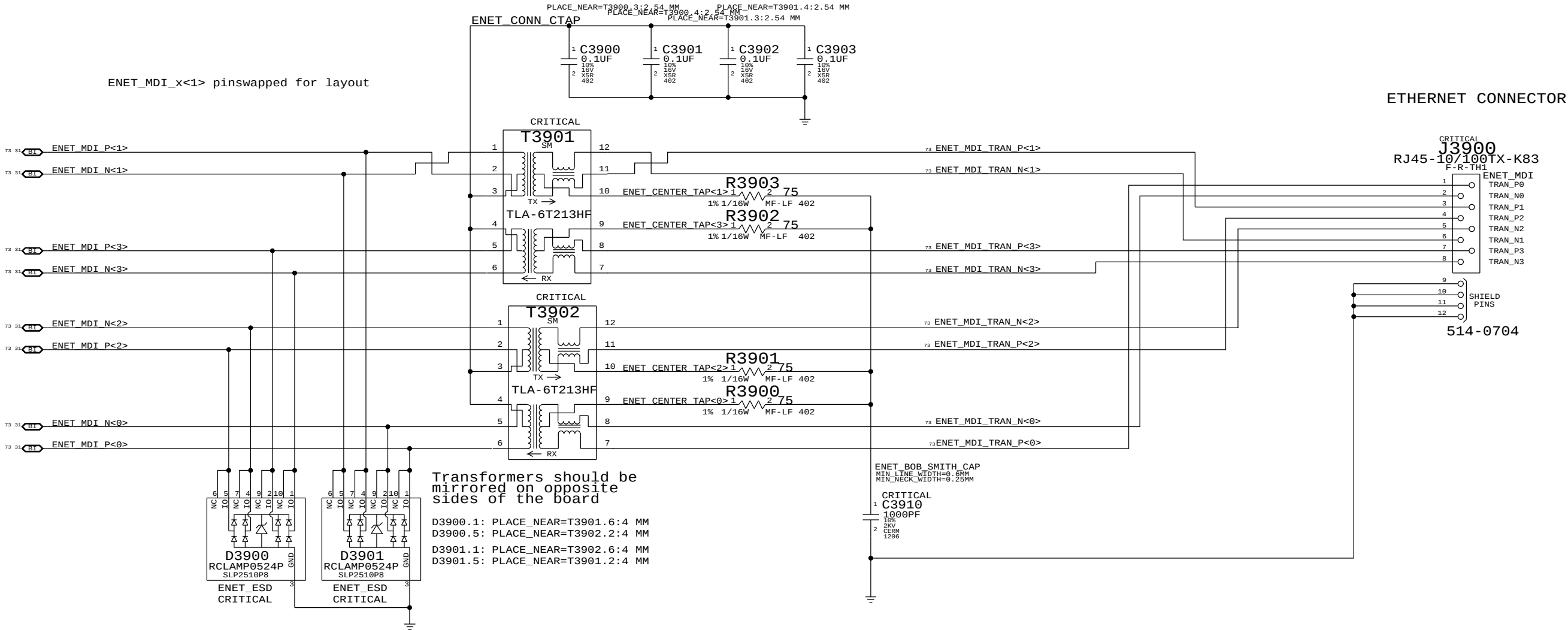
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- COPY THIS PAGE FROM K36 CSA.39



DO NOT SYNC FROM K6, WITH K84'S CONNECTOR

SYNC MASTER=K87 MLB SYNC DATE=02/26/2010

ETHERNET CONNECTOR

Apple Inc.

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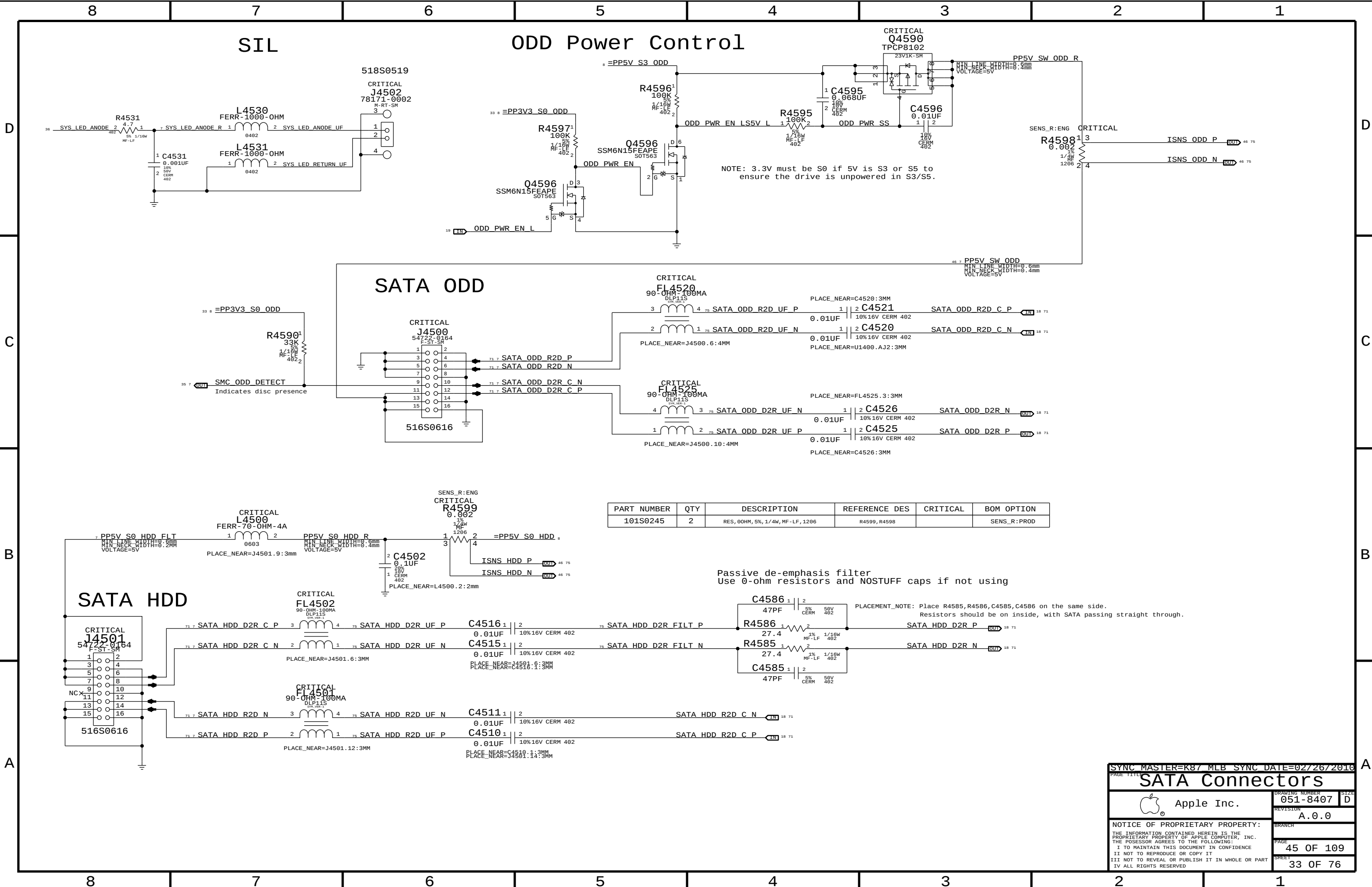
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	2	RES, 00HM, 5%, 1/4W, MF-LF, 1206	R4599, R4598		SENS_R:PROD

Passive de-emphasis filter
Use 0-ohm resistors and N0STUFF caps if not using

SYNC MASTER=K87 MLB SYNC DATE=02/26/2010

SATA Connectors

Apple Inc.

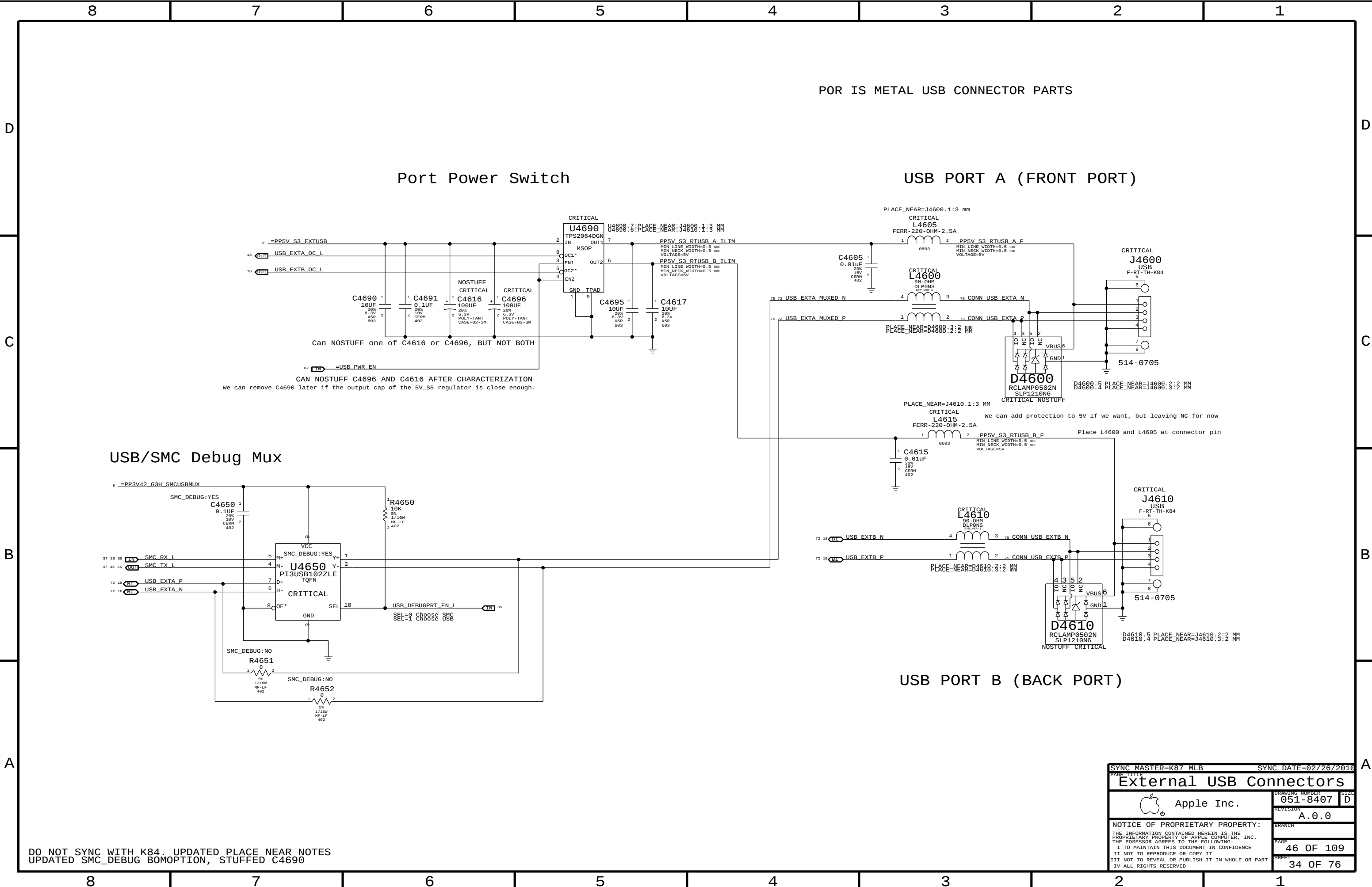
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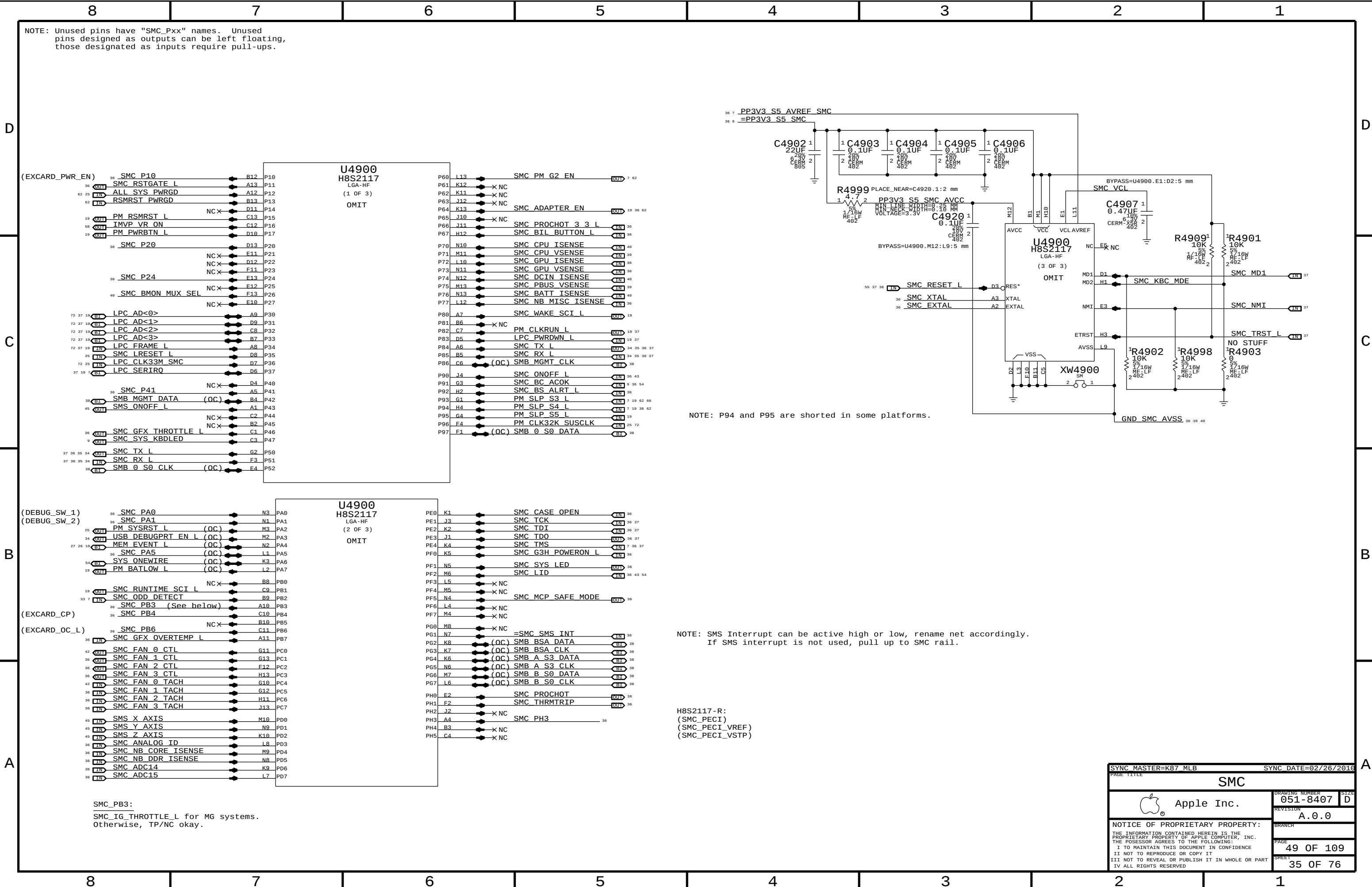
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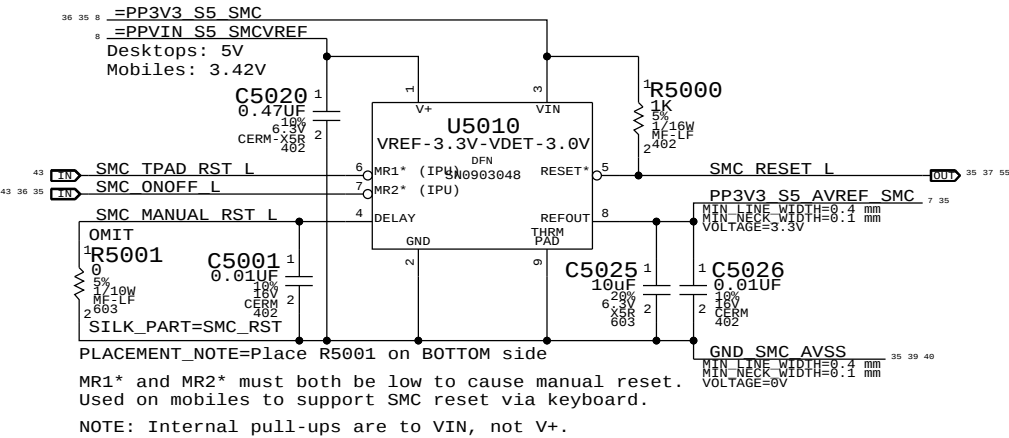


DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES
UPDATED SMC_DEBUG_BOMOPTION, STUFFED C4690

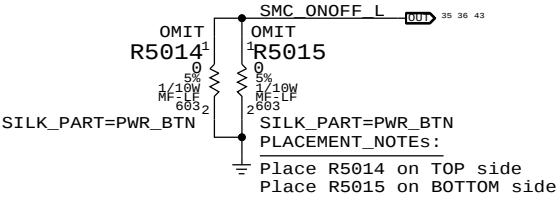
SYNC MASTER=K87_MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8407
		SIZE	D
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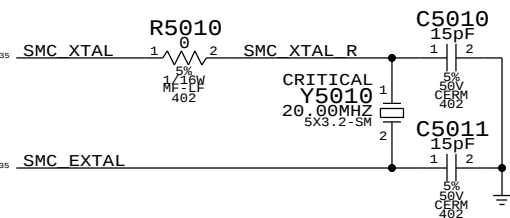
SMC Reset "Button", Supervisor & AVREF Supply



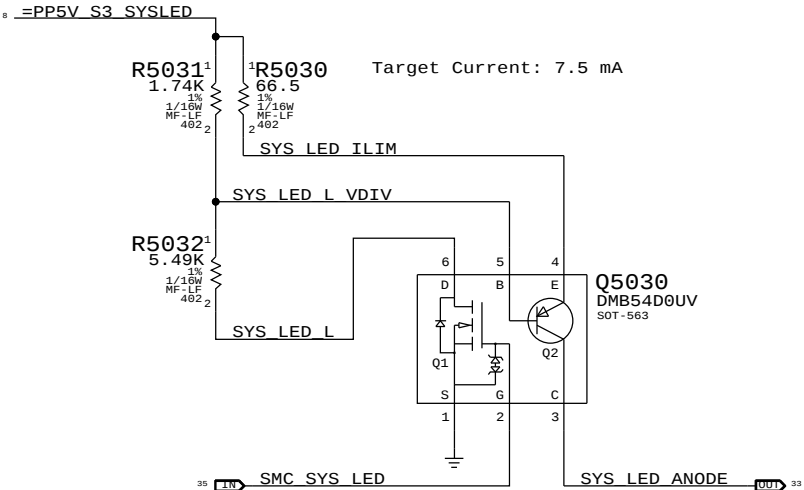
Debug Power "Buttons"



SMC Crystal Circuit

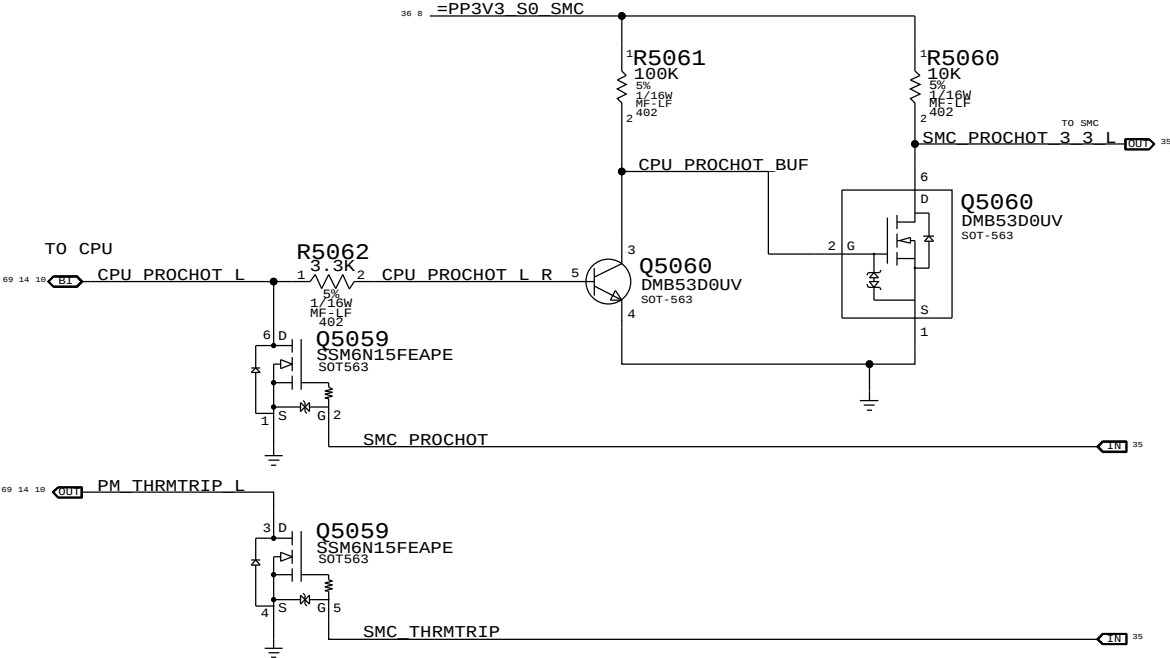


System (Sleep) LED Circuit

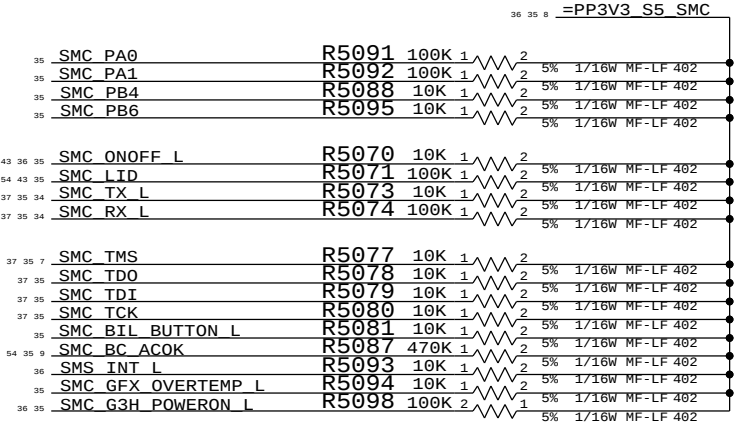


R5030,R5031,R5032 CHANGED FOR DIMMER LED

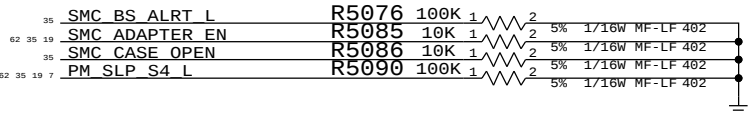
SMC FSB to 3.3V Level Shifting



SMC Pull-ups

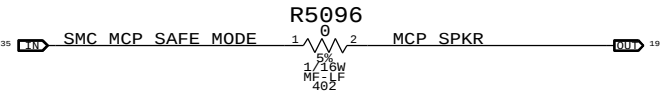


SMC Pull-downs



SMC Aliases

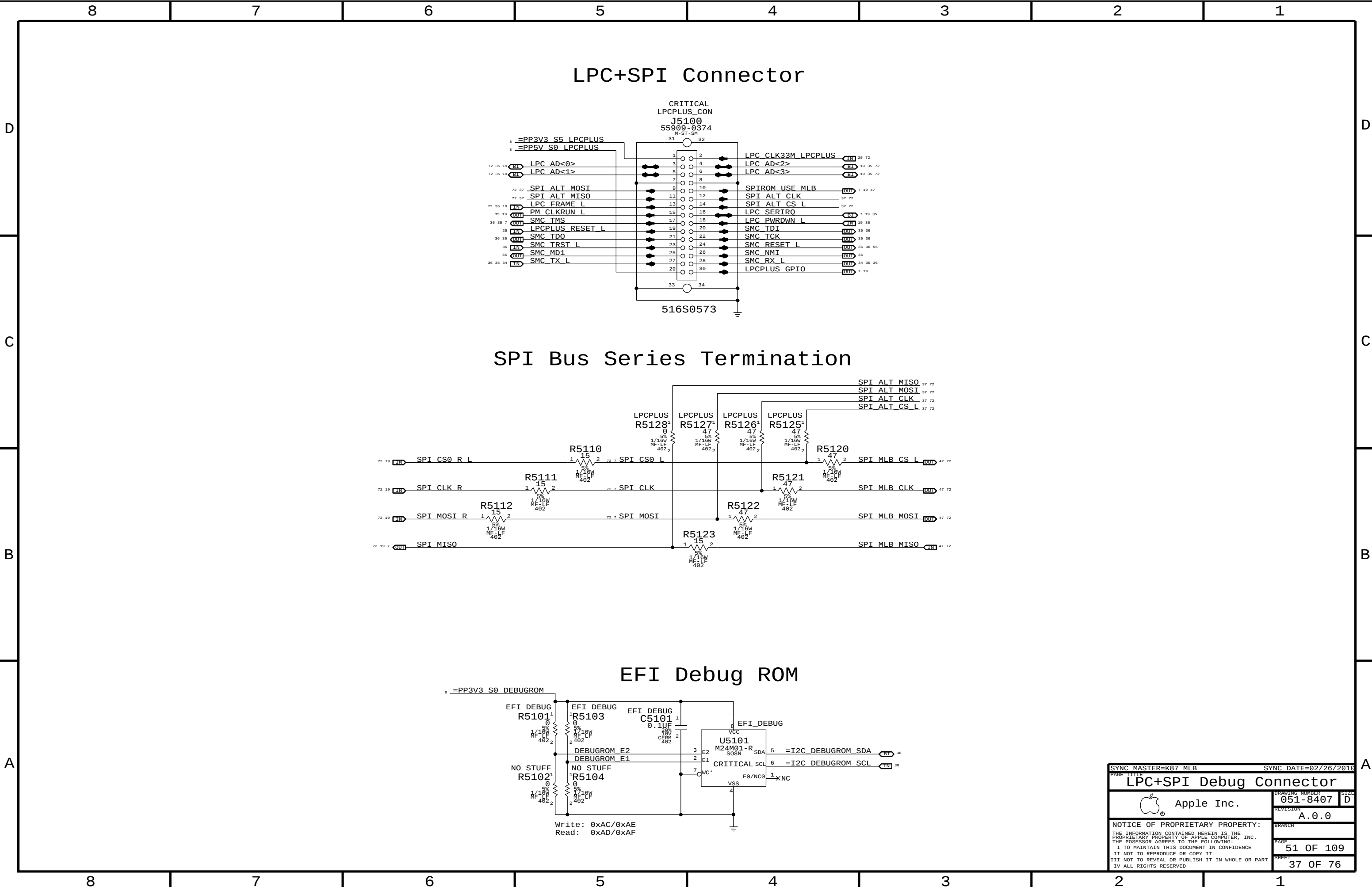
SMC MCP VSENSE	=	SMC ADC14
SMC CPU FSB ISENSE	=	SMC ADC15
SMC MCP CORE ISENSE	=	SMC NB CORE ISENSE
SMC MCP DDR ISENSE	=	SMC NB DDR ISENSE
TP SMC CPU HI ISENSE	=	SMC NB MISC ISENSE
TP SMC GPU 1V8 ISENSE	=	SMC ANALOG ID
TP SMC GPU ISENSE	=	SMC GPU ISENSE
TP SMC GPU VSENSE	=	SMC GPU VSENSE
SMC GFX THROTTLE L	=	SMC IG THROTTLE L
SMS INT L	=	=SMC SMS INT
MCP WAKE REQ L	=	SMC G3H POWERON L

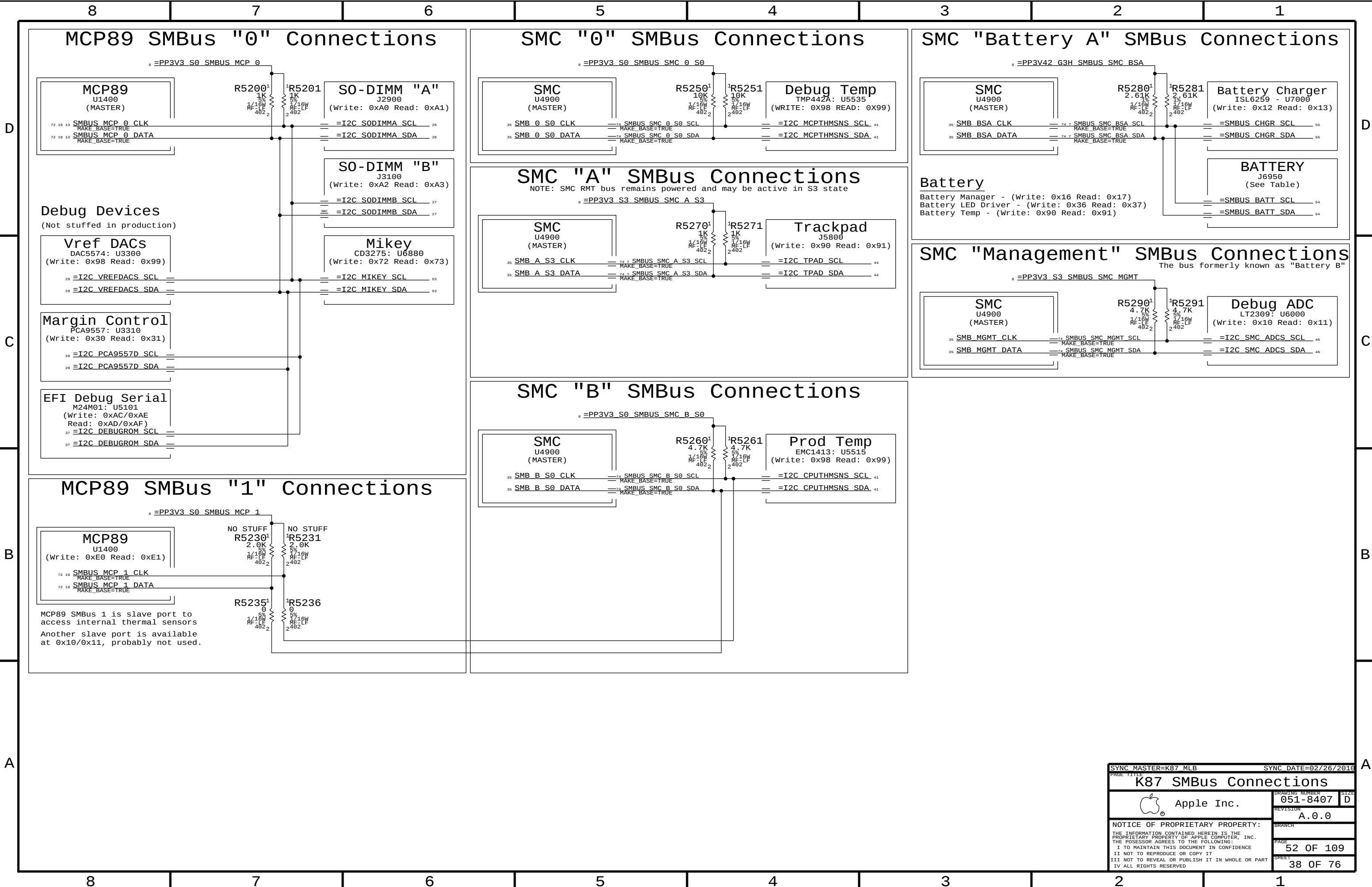


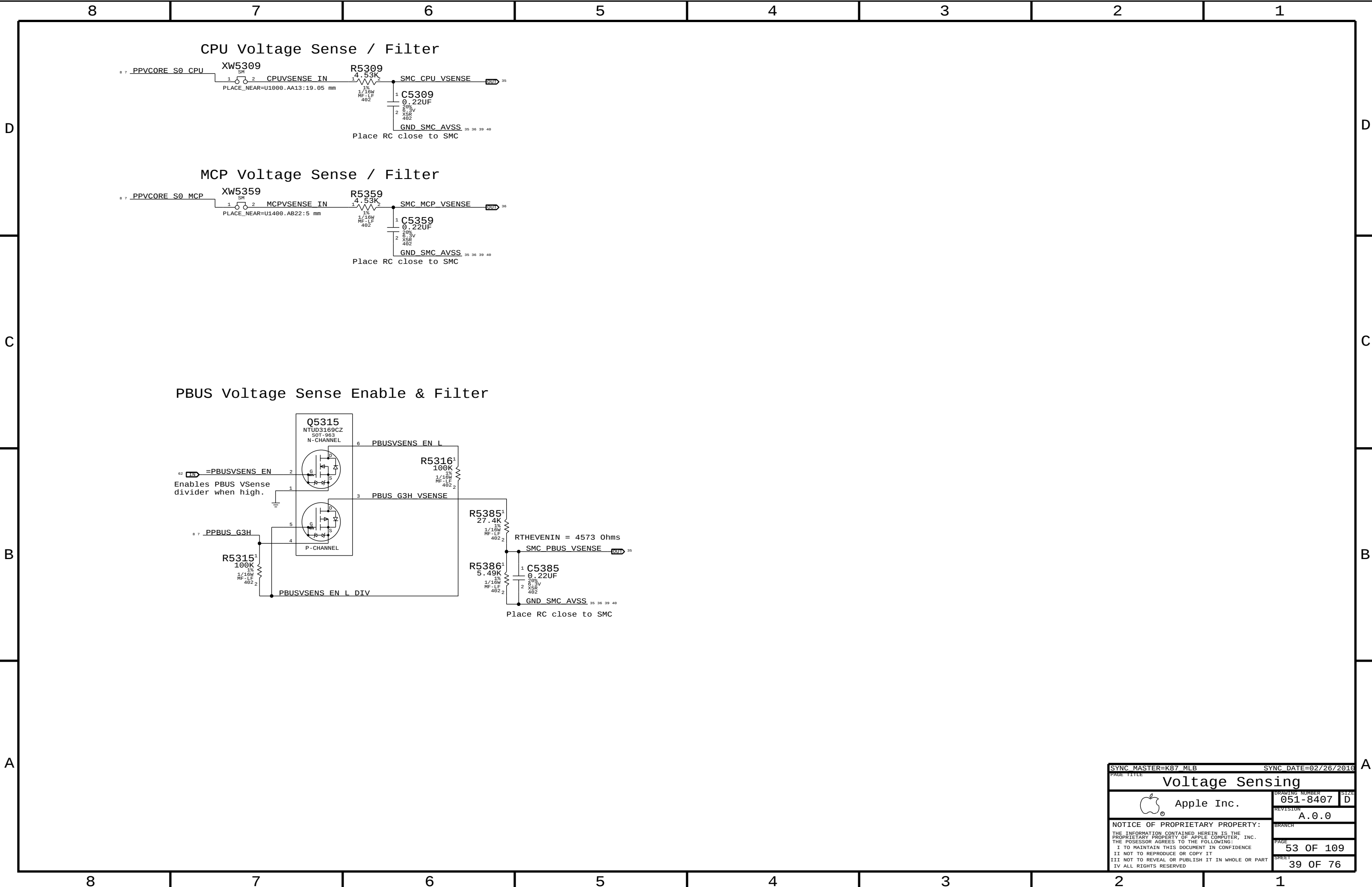
Unused Pins

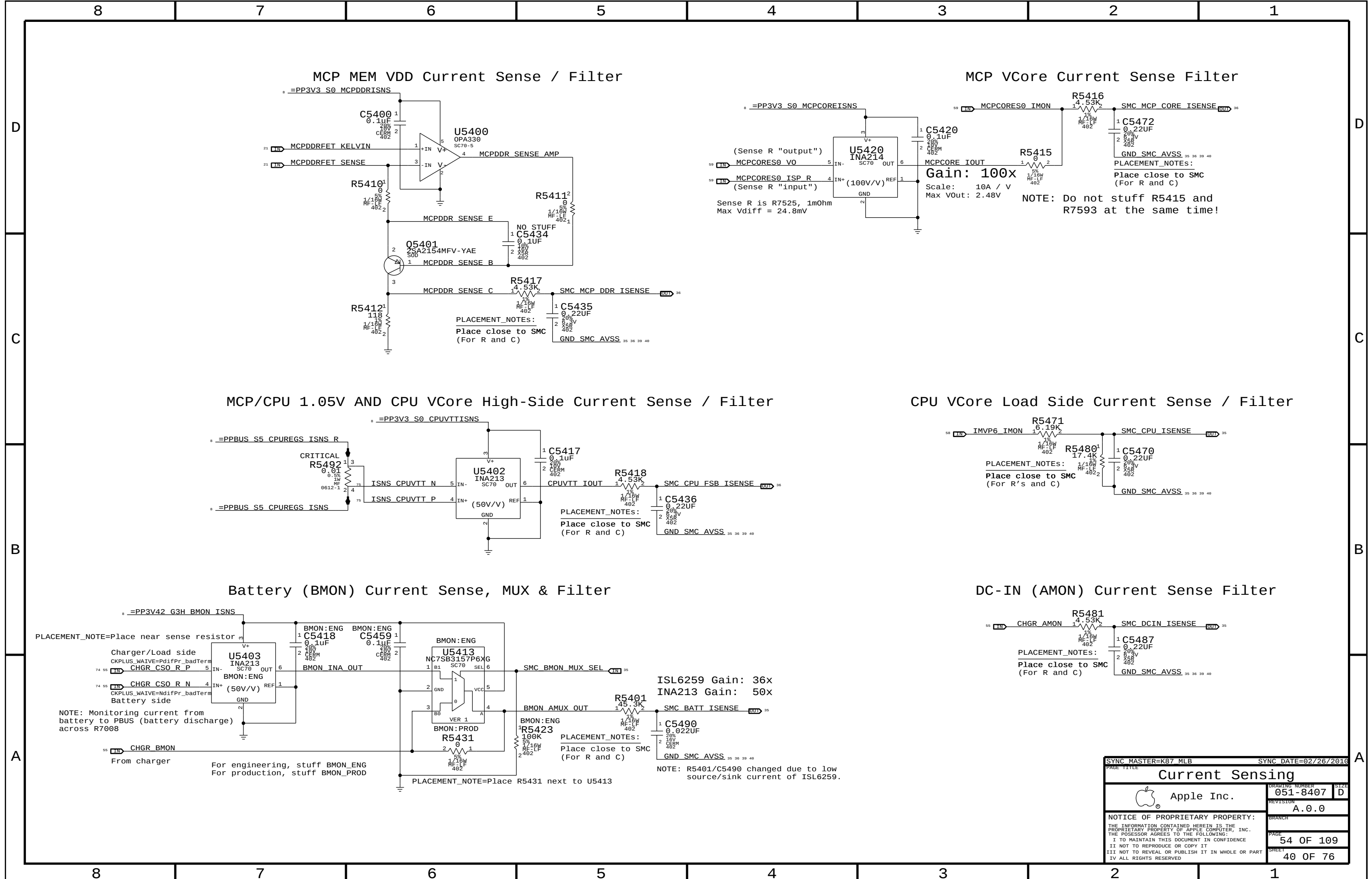
SMC FAN 1 CTL	=	TP SMC FAN 1 CTL
TP SMC FAN 1 TACH	=	SMC FAN 1 TACH
SMC FAN 2 CTL	=	NC SMC FAN 2 CTL
NC SMC FAN 2 TACH	=	SMC FAN 2 TACH
SMC FAN 3 CTL	=	NC SMC FAN 3 CTL
NC SMC FAN 3 TACH	=	SMC FAN 3 TACH
SMC_RSTGATE_L	=	TP SMC_RSTGATE_L
SMC_P10	=	TP SMC_P10
SMC_P20	=	TP SMC_P20
SMC_P24	=	TP SMC_P24
SMC_P41	=	TP SMC_P41
SMC_PB3	=	TP SMC_PB3
SMC_PH3	=	TP SMC_PH3

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
SMC Support		DRAWING NUMBER	
Apple Inc.		051-8407	
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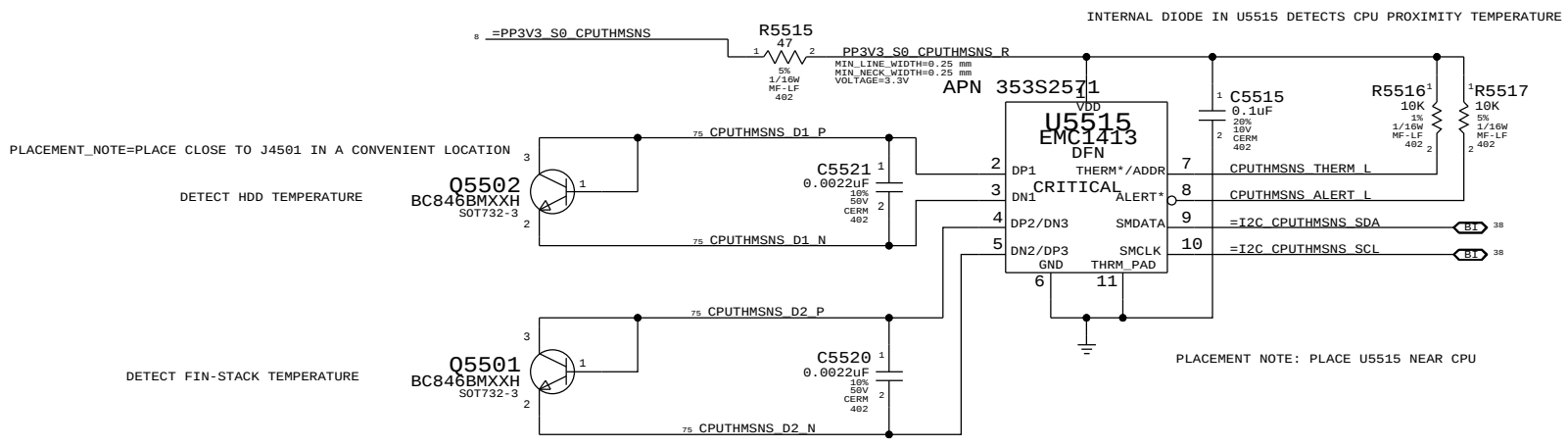




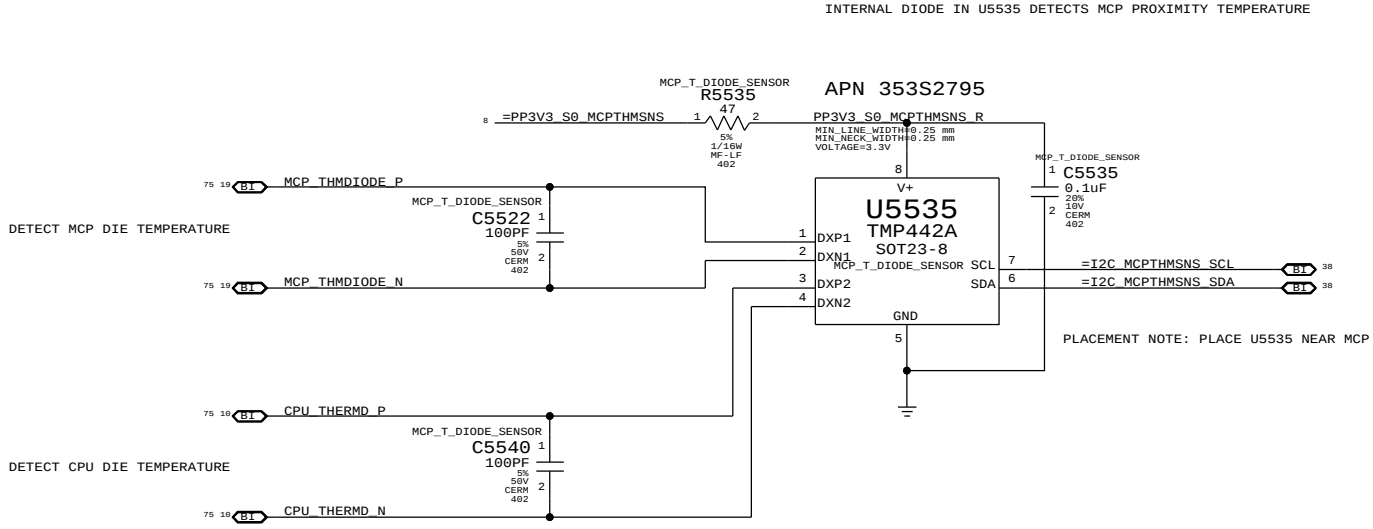


SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE		Current Sensing	
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CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR

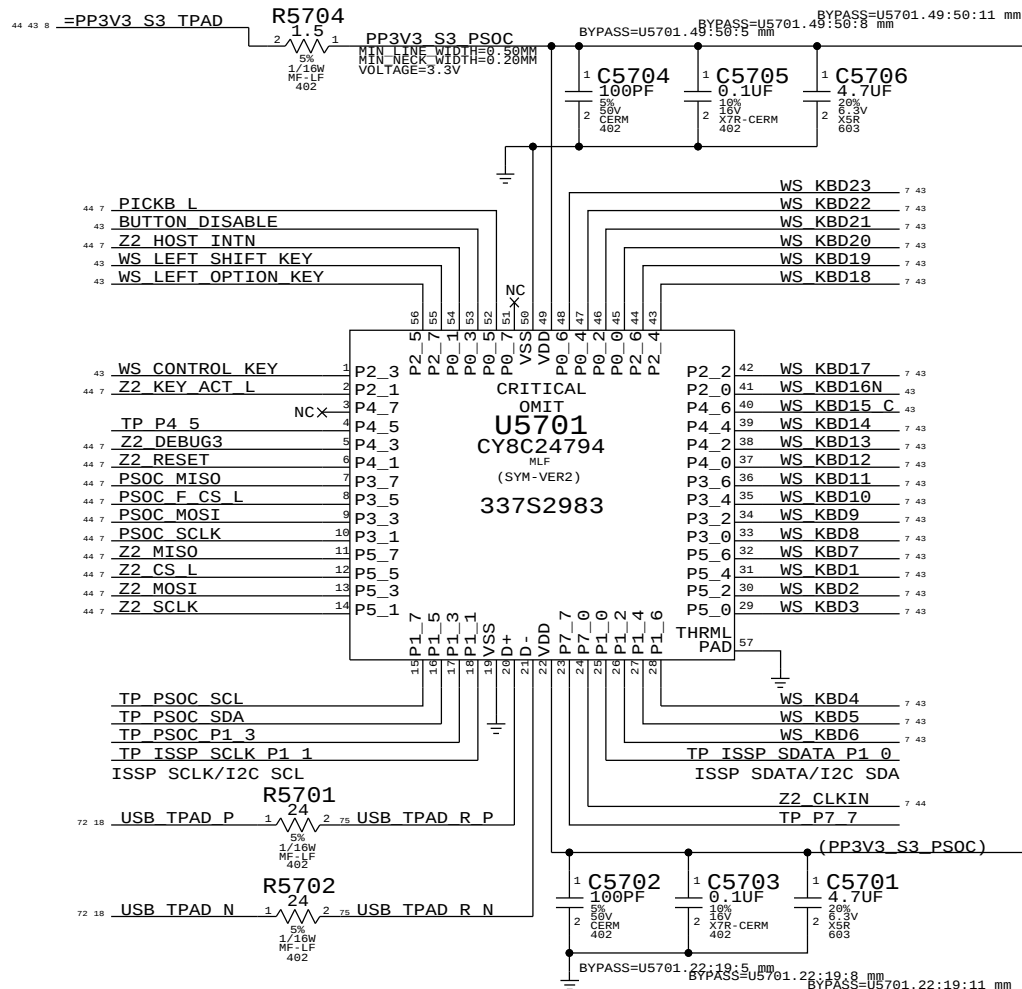


MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR

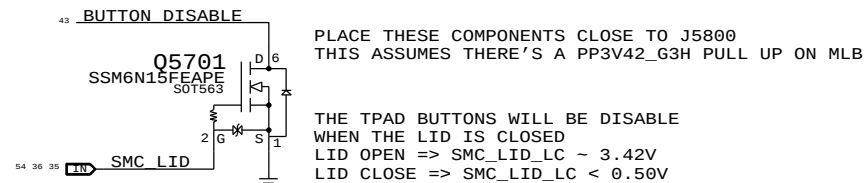


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

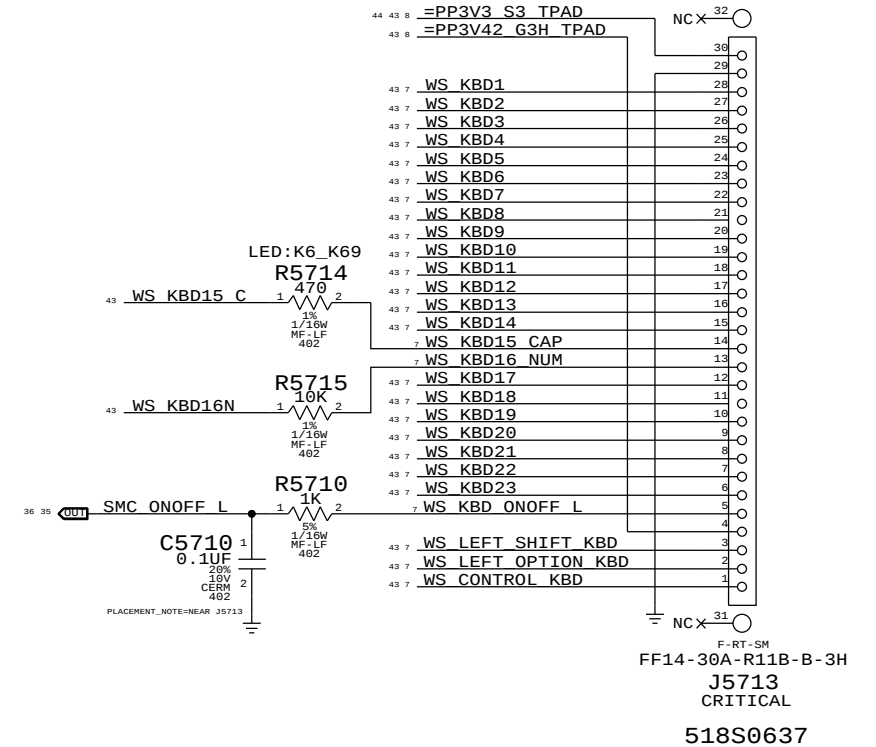


TPAD Buttons Disable



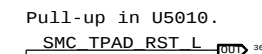
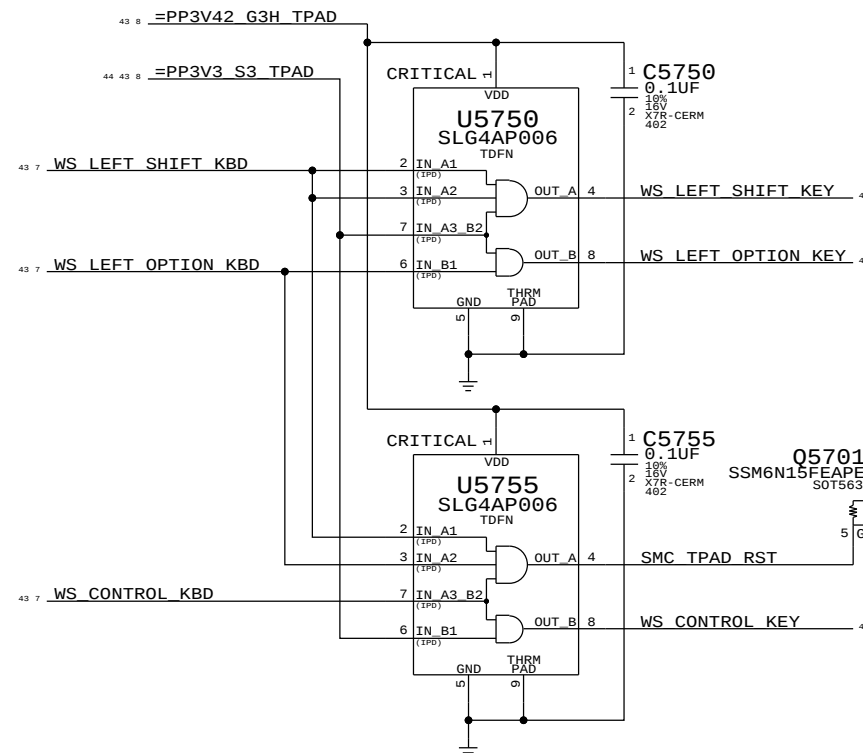
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



SMC Manual Reset & Isolation

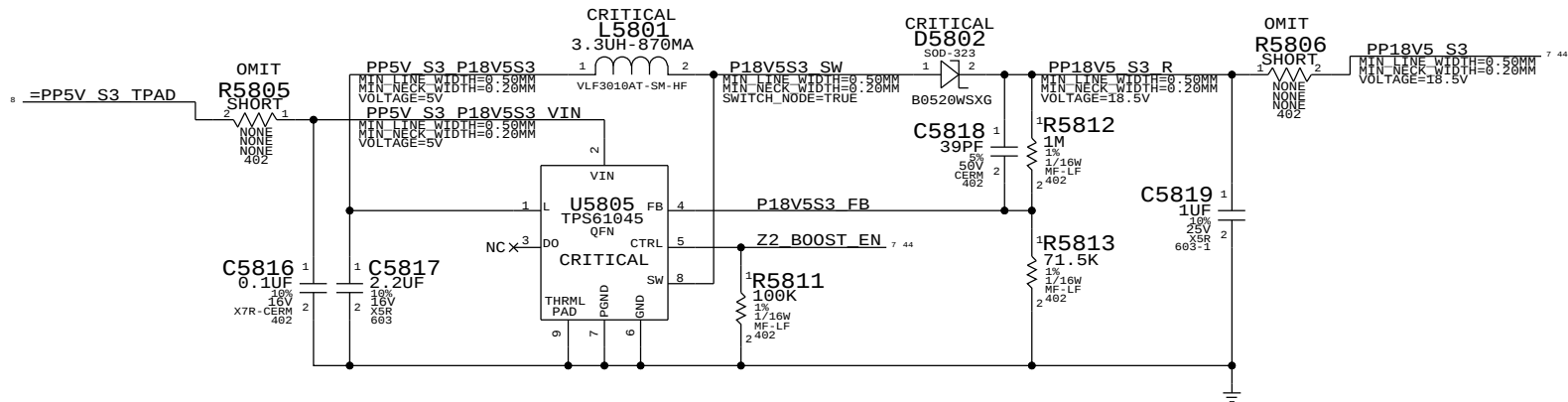
Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



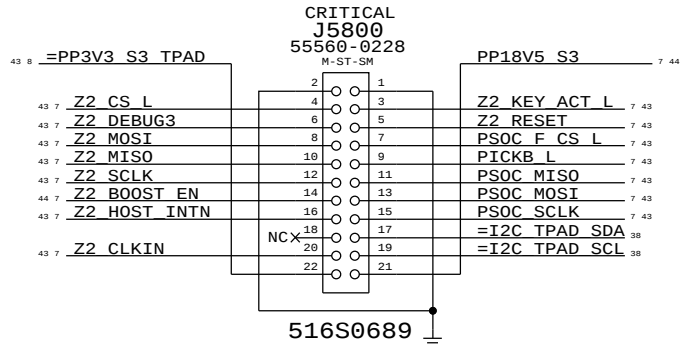
SYNC MASTER=K87 MLB		SYNC DATE=02/26/2010	
PAGE TITLE			
WELLSPRING 1			
	Apple Inc.		DRAWING NUMBER
			051-8407
		SIZE	D
		REVISION	
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		SHEET	
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BOOSTER +18.5VDC FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED

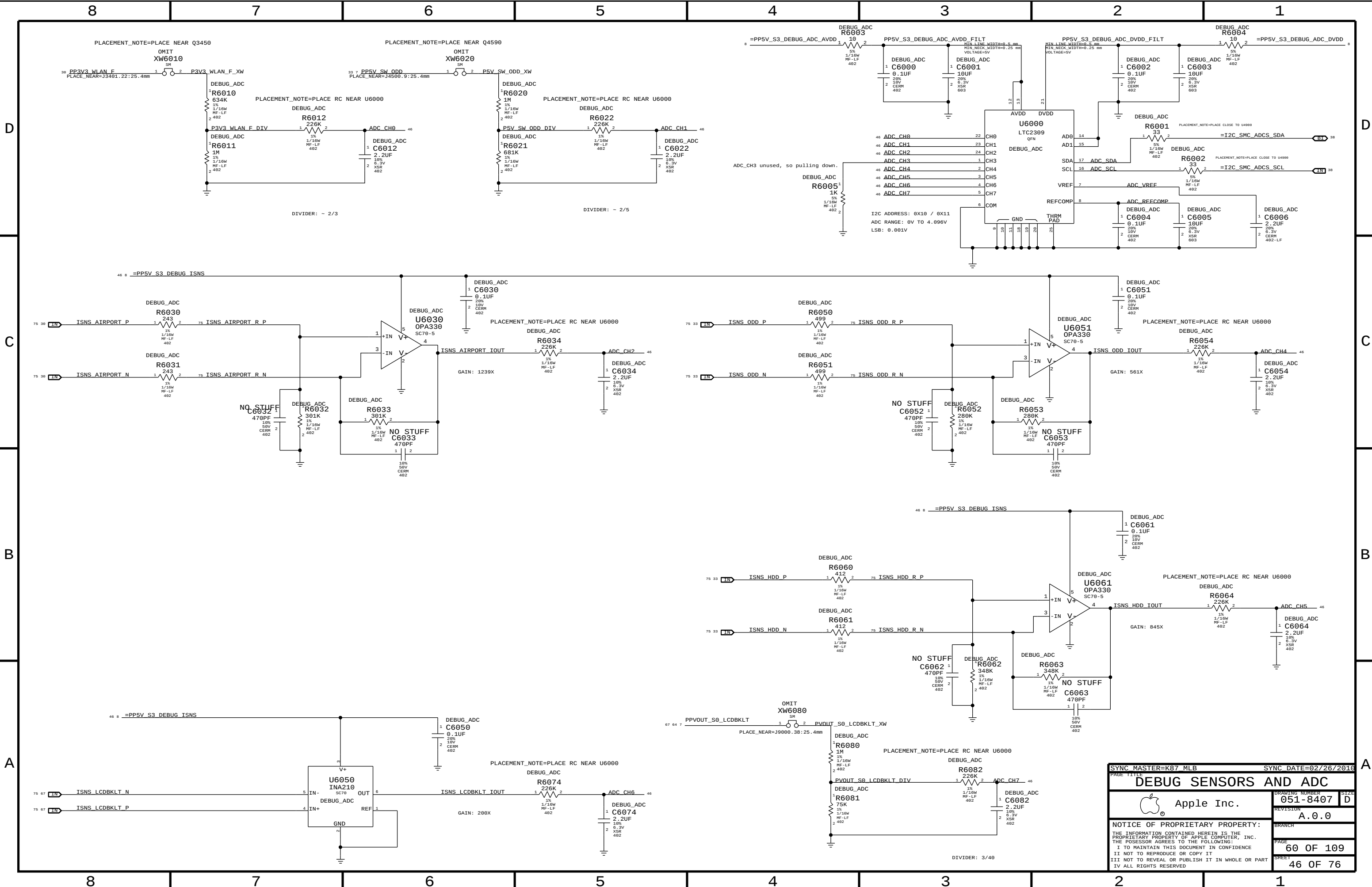


IPD Flex Connector



DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

SYNC MASTER=K87_MLB		SYNC DATE=02/26/2016	
PAGE TITLE		WELLSPRING 2	
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SYNC MASTER=K87 MLB

SYNC DATE=02/26/2016

051-8407

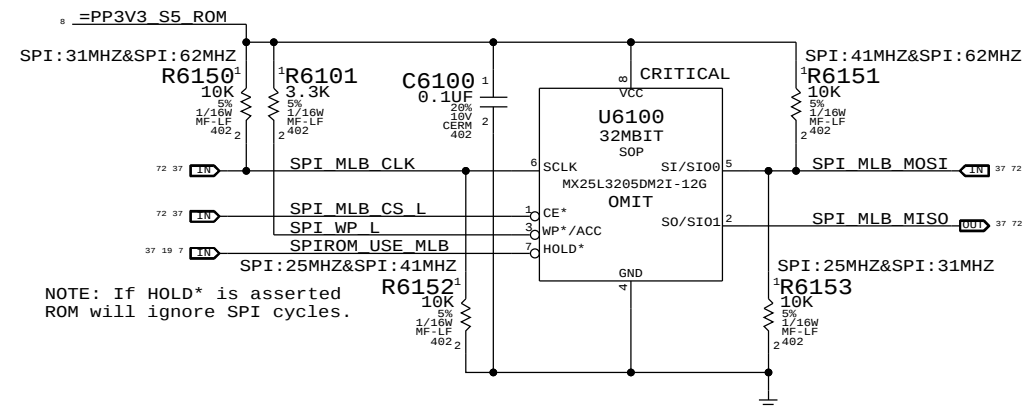
A.0.0

60 OF 109

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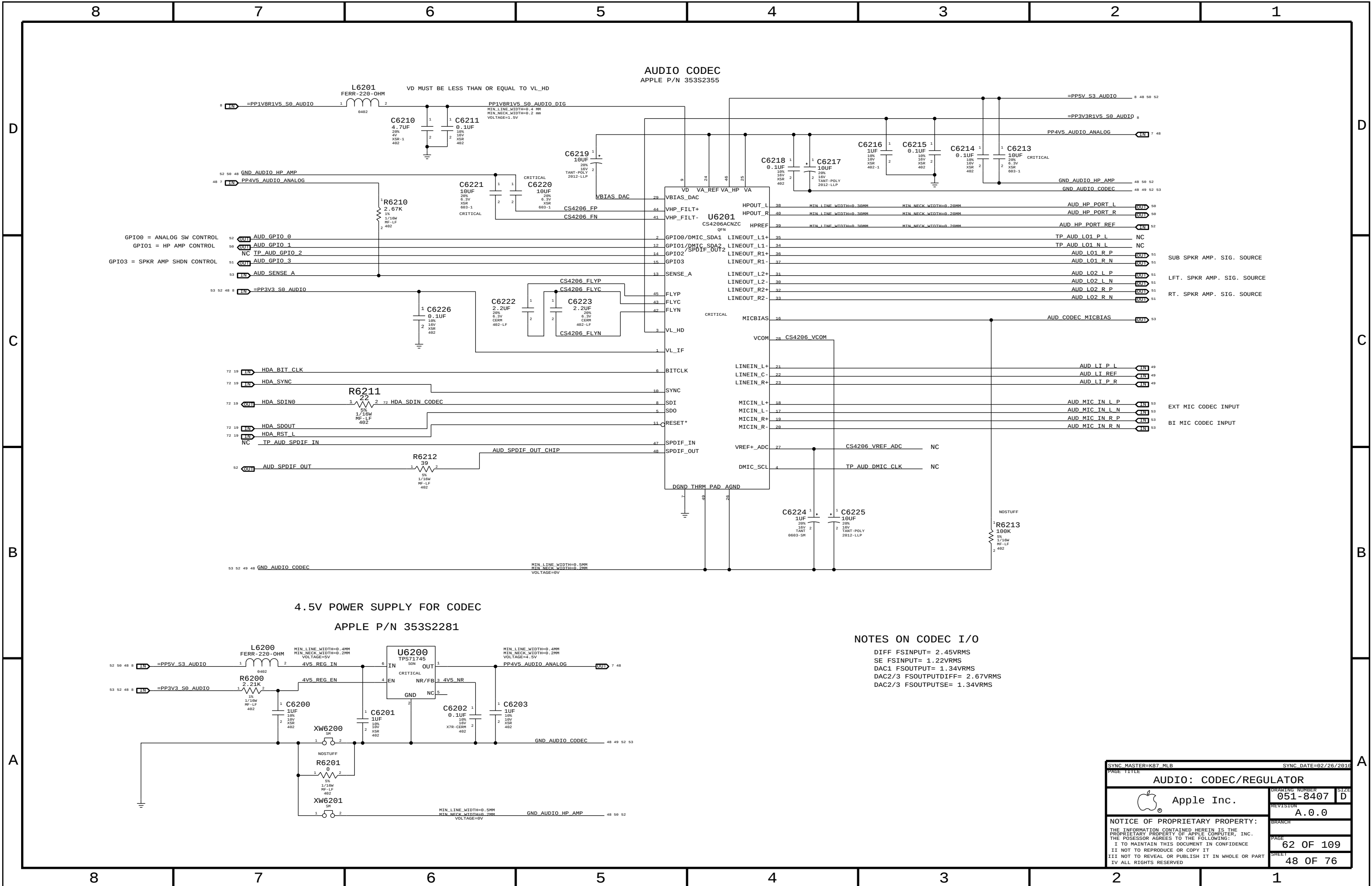
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Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

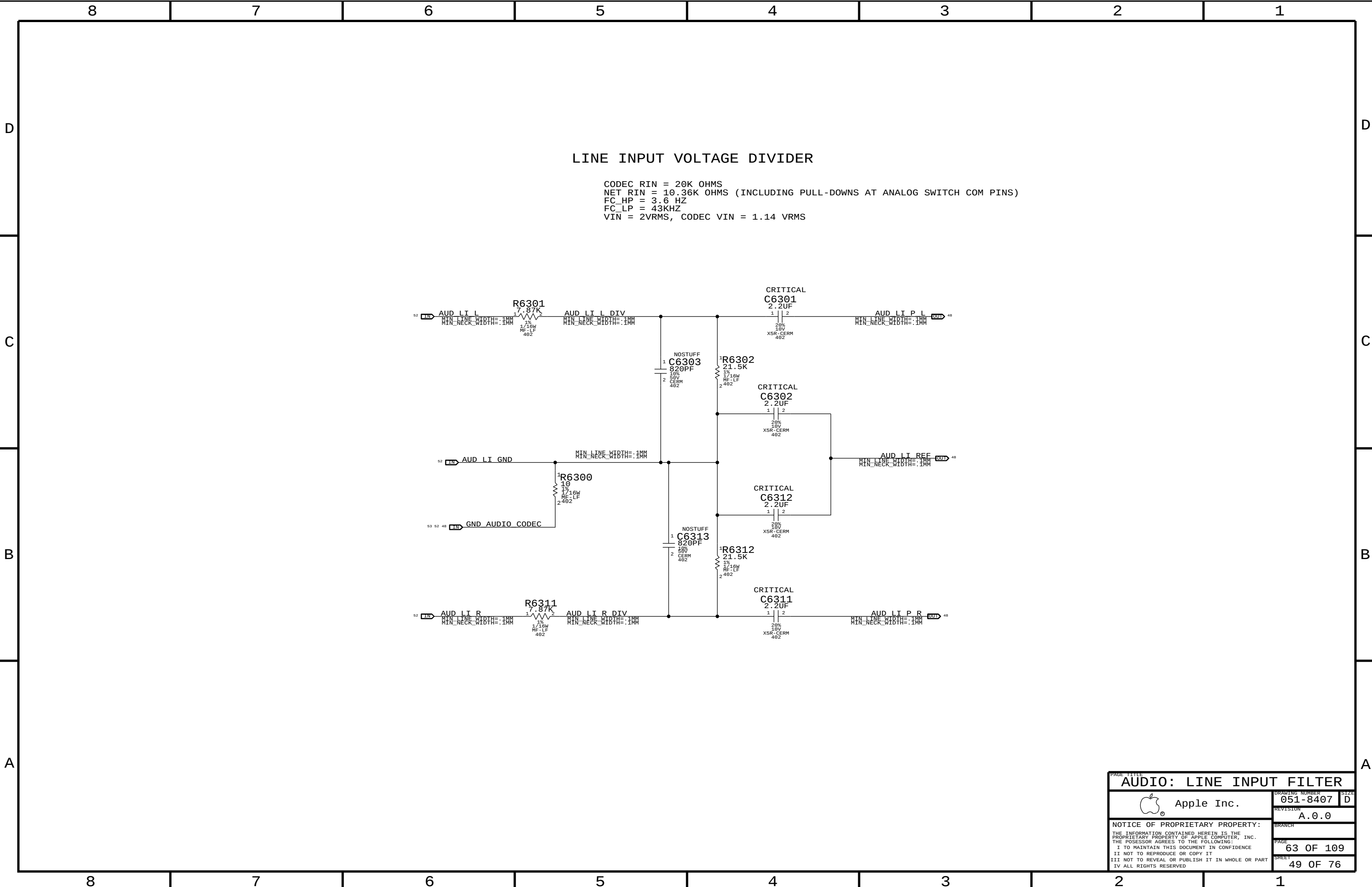
NOTE: 42 & 62 MHz use FAST_READ command.



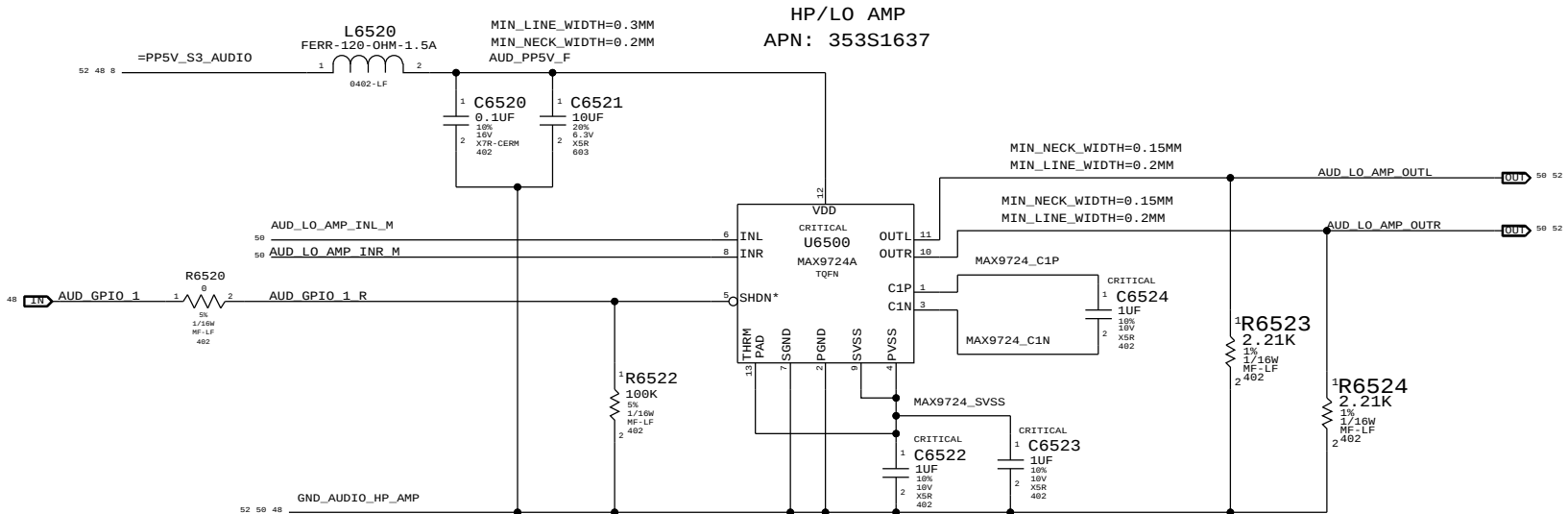
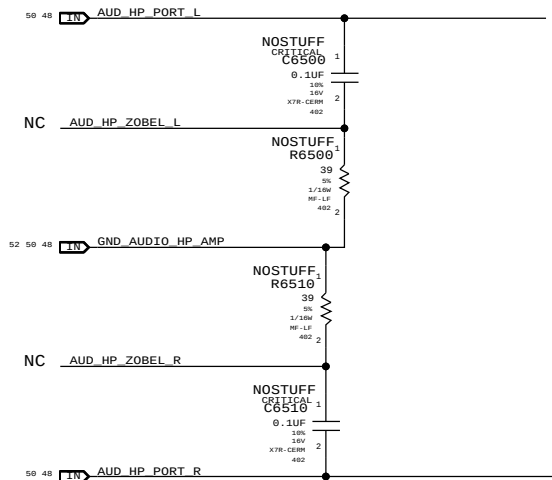
NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2010	
PAGE TITLE		AUDIO: CODEC/REGULATOR	
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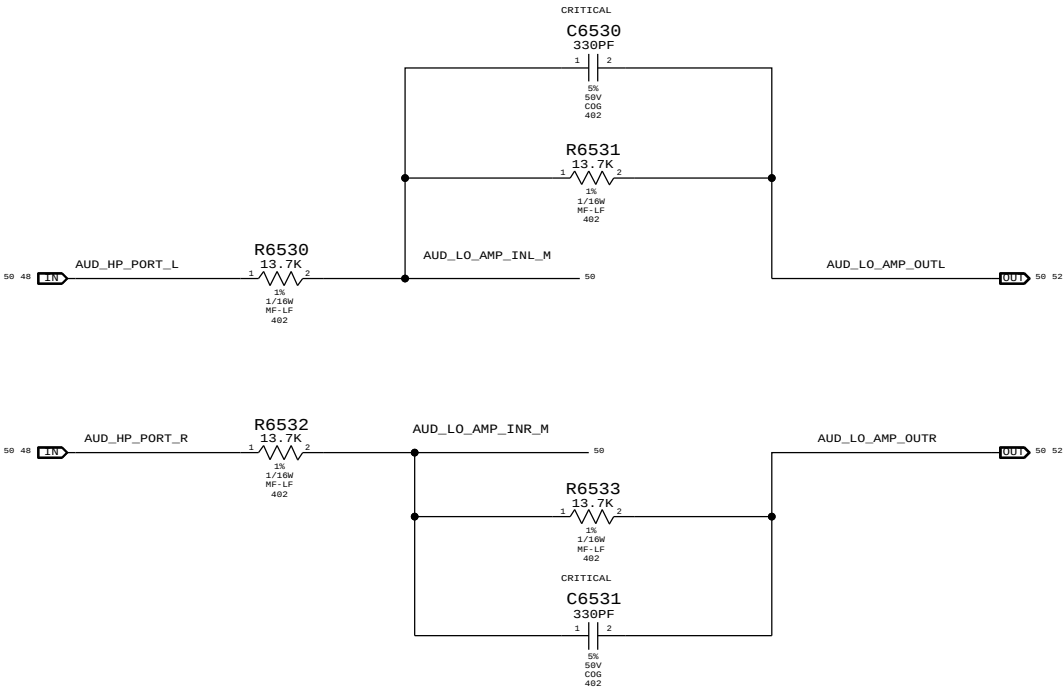


CS4206 HP OUTPUT ZOBEL NETWORK



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ

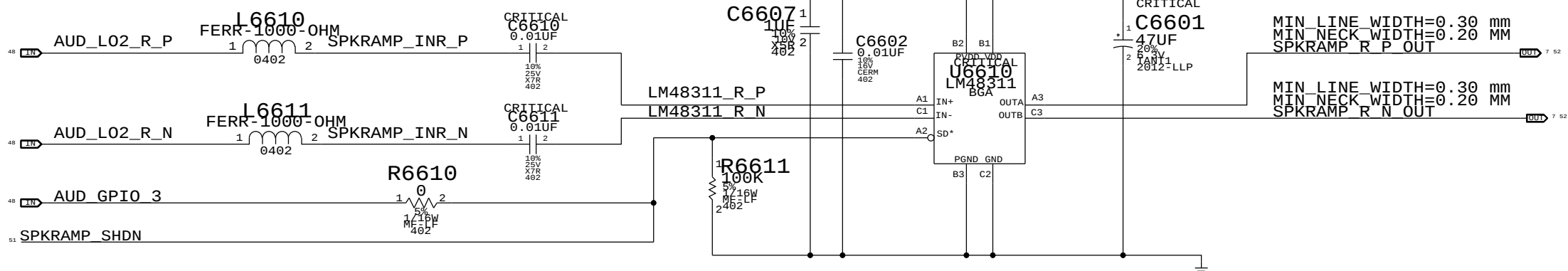


SYNC MASTER=K87 MLB		SYNC DATE=02/26/2010	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
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SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRK AMP. INPUT REFERRED CLIP POINT = --6dBFS

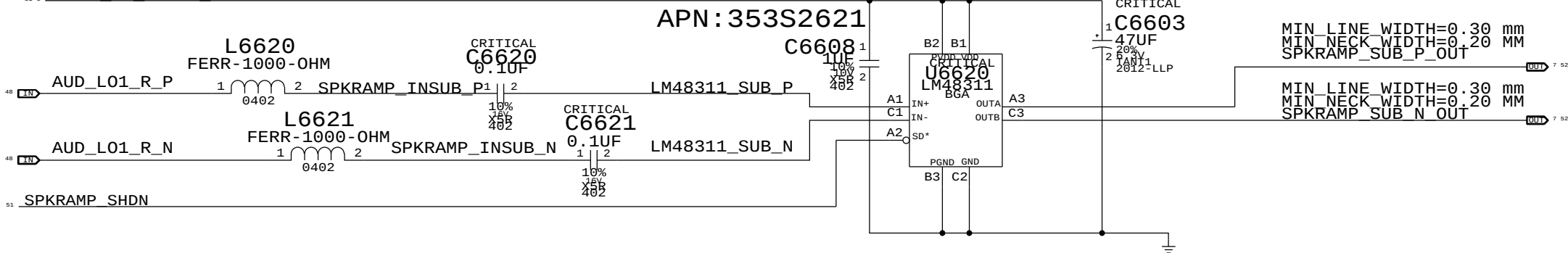
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

51 8 =PP5V_S3_AUDIO_AMP



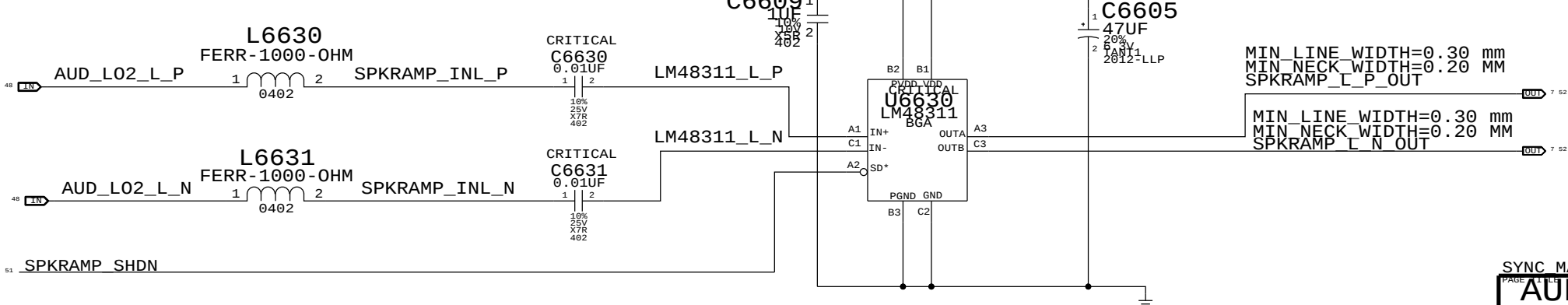
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

51 8 =PP5V_S3_AUDIO_AMP



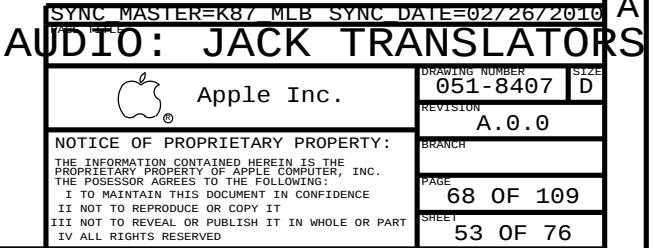
51 8 =PP5V_S3_AUDIO_AMP

ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM



PAGE 1 OF 1 SYNC MASTER=K87 MLB SYNC DATE=02/26/2010

AUDIO0: SPEAKER AMP		
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D



C

C



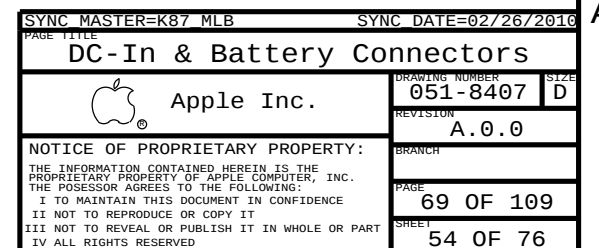
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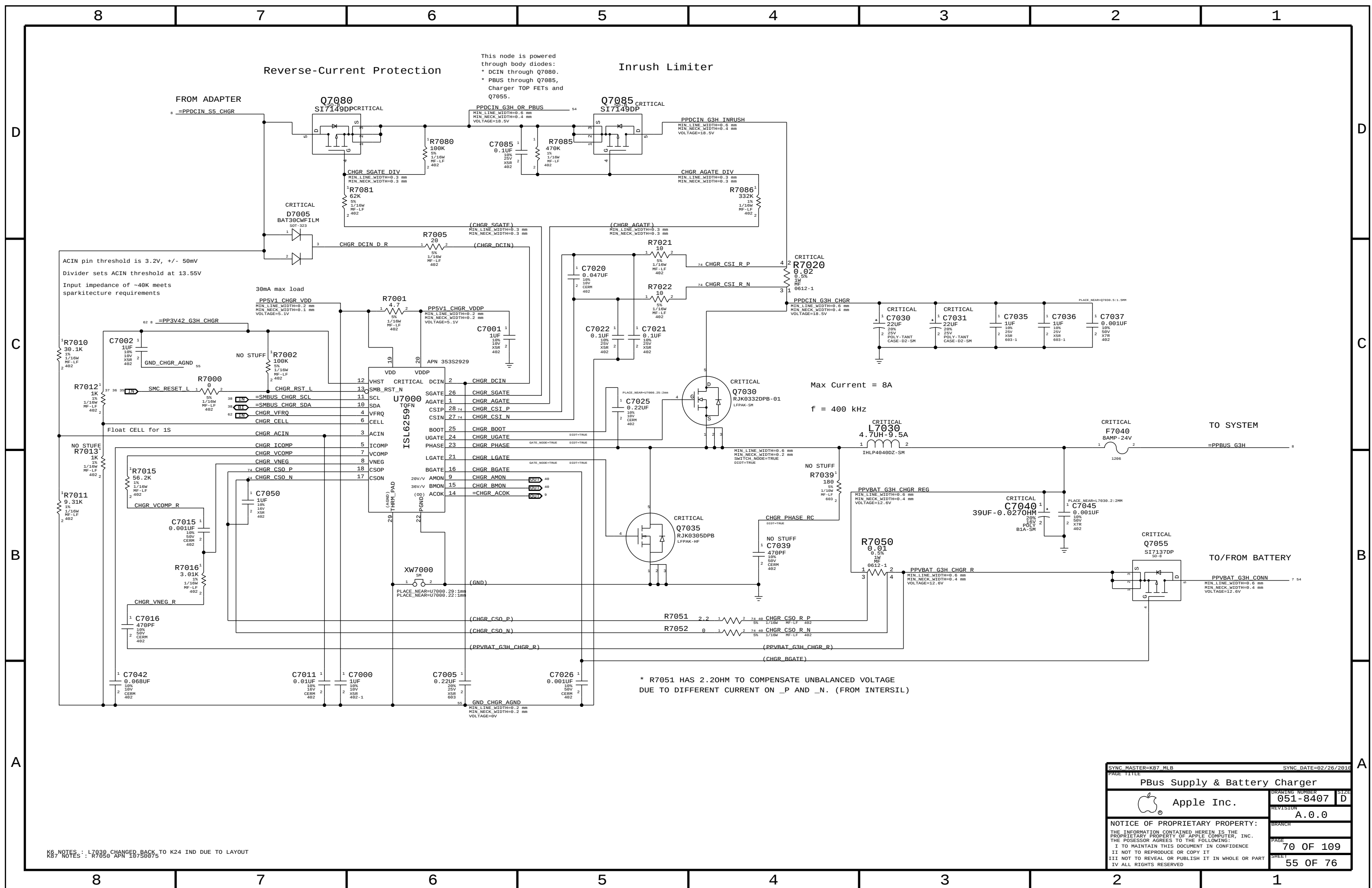
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6831	1	SUB ASSY - HALL EFFECT, K86 K87	J6955	CRITICAL	



A

A



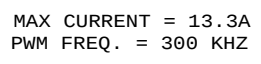


5V_S3/3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$

$$V_{OUT} = (2 * RC / RD) + 2$$



PWM FREQ. = 375 KHZ
MAX CURRENT = 9.1A

NOTE: DONT SYNC THIS PAGE FROM T27

SEPERATED MASTER PG00D FOR BOTH 5V AND 3V3.

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016		A
PAGE TITLE				
5V/3.3V SUPPLY				
 Apple Inc.		DRAWING NUMBER		SIZE
		051-8407		D
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D



B

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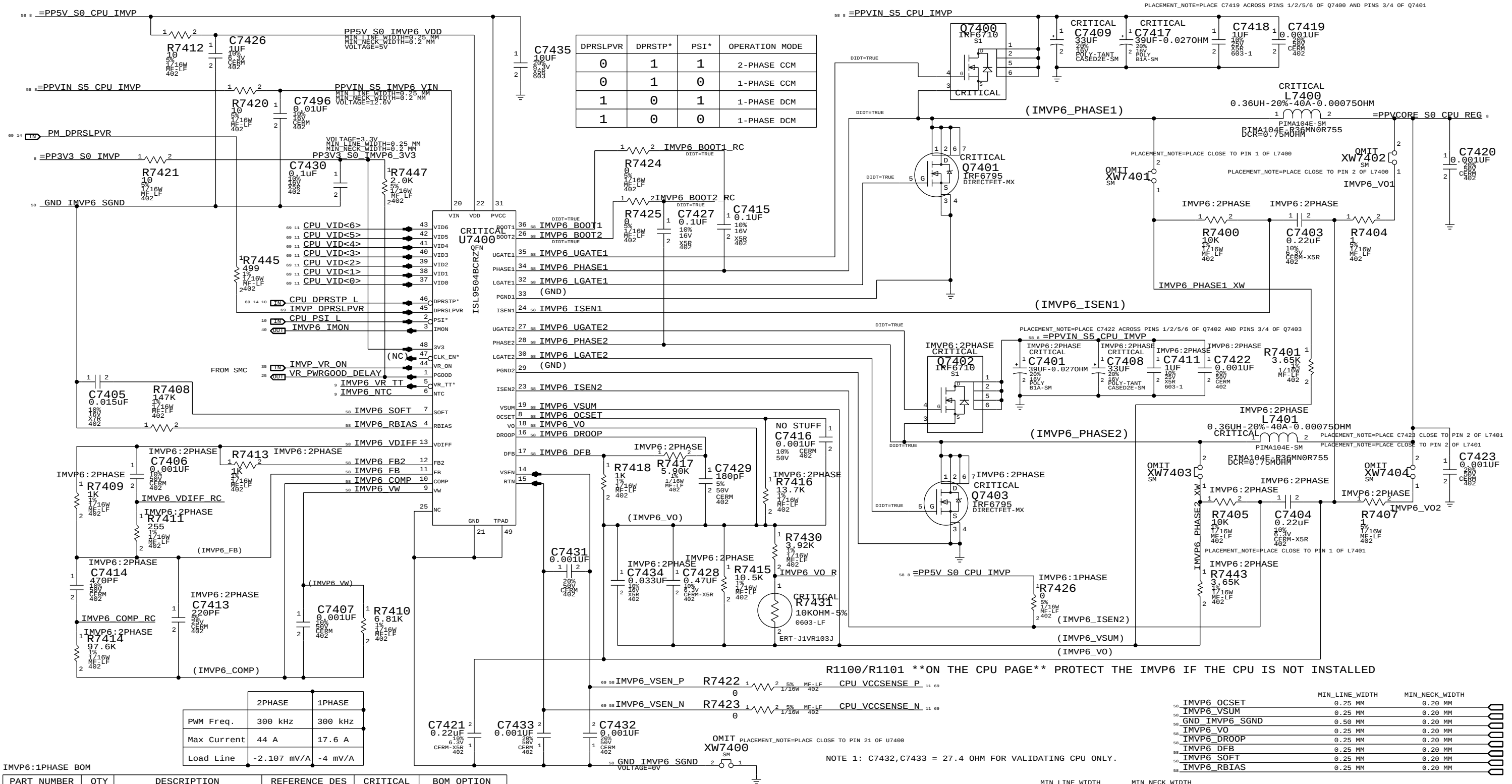
D

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IMVP6 CPU VCORE REGULATOR



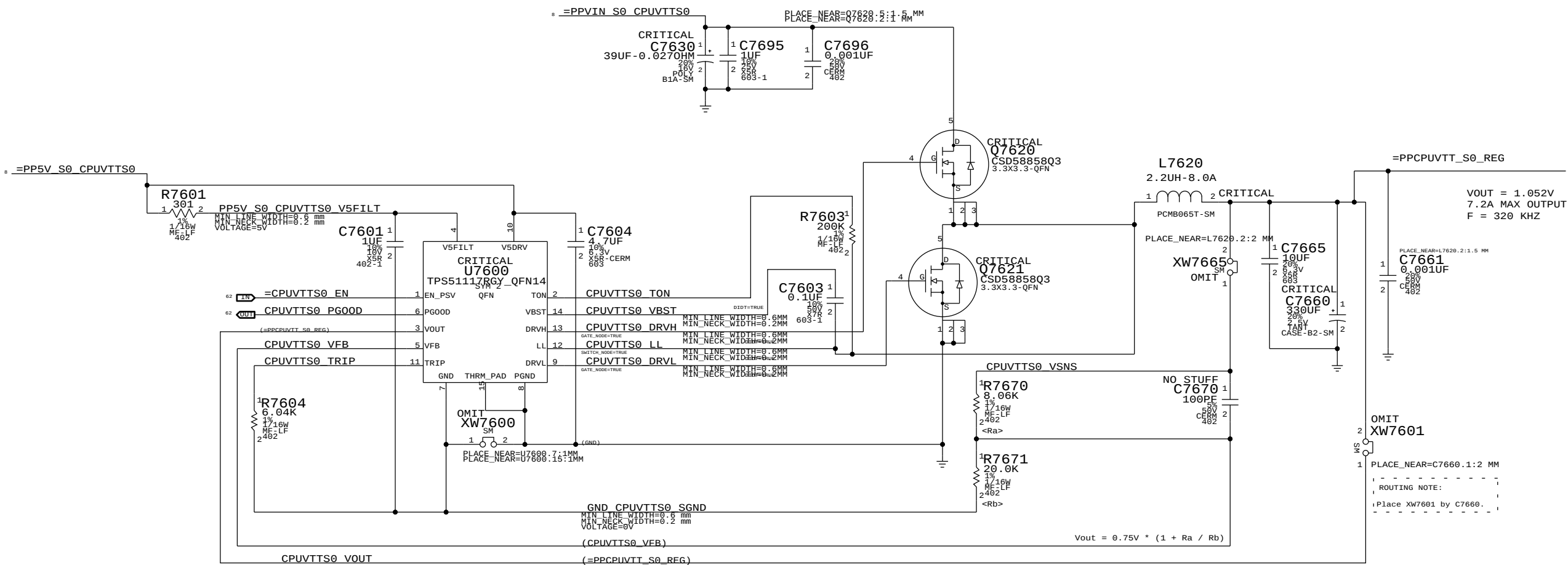
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11450307	1	RES,MTL FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
11450336	1	RES,MTL FILM,1/16W, 10.9K, 1,0402,SM,LF	R7416		IMVP6:1PHASE
13250080	1	CAP,CER.,22UF,20,6.3V,X5R,0402	C7428		IMVP6:1PHASE
11450236	1	RES,MTL FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
11450160	1	RES,MTL FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
13254720	1	CAP CER 470PF,+/-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
11450410	1	RES,MTL FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
13250045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
13151027	1	CAP,CER,100PF,5K,50V,CC0402	C7413		IMVP6:1PHASE

		MIN. LINE WIDTH	MIN. NECK WIDTH
58	IMVP6_VDIFF	0.25 MM	0.20 MM
58	IMVP6_FB2	0.25 MM	0.20 MM
58	IMVP6_FB	0.25 MM	0.20 MM
58	IMVP6_COMP	0.25 MM	0.20 MM
58	IMVP6_VW	0.25 MM	0.25 MM
69	IMVP6_VSEN_P	0.25 MM	0.25 MM
69	IMVP6_VSEN_N	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
58 IMVP6_PHASE1	1.5 MM	0.25 MM	
58 IMVP6_B00T1	0.25 MM	0.25 MM	
58 IMVP6_UGATE1	1.5 MM	0.25 MM	
58 IMVP6_LGATE1	1.5 MM	0.25 MM	
58 IMVP6_ISEN1	0.25 MM	0.25 MM	
	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
58 IMVP6_PHASE2	1.5 MM	0.25 MM	
58 IMVP6_B00T2	0.25 MM	0.25 MM	
58 IMVP6_UGATE2	0.25 MM	0.25 MM	
58 IMVP6_LGATE2	0.25 MM	0.25 MM	
58 IMVP6_ISEN2	0.25 MM	0.25 MM	

SYNCH MASTER-K87 MLB		SYNCH DATE=02/26/201	
PAGE TITLE			
IMVP6 CPU VCore Regulator			
		DRAWING NUMBER	
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CPUVTT POWER SUPPLY



SYNC MASTER=K87_MLB		SYNC DATE=02/26/2016	
PAGE TITLE		CPU VTT(1.05V) SUPPLY	
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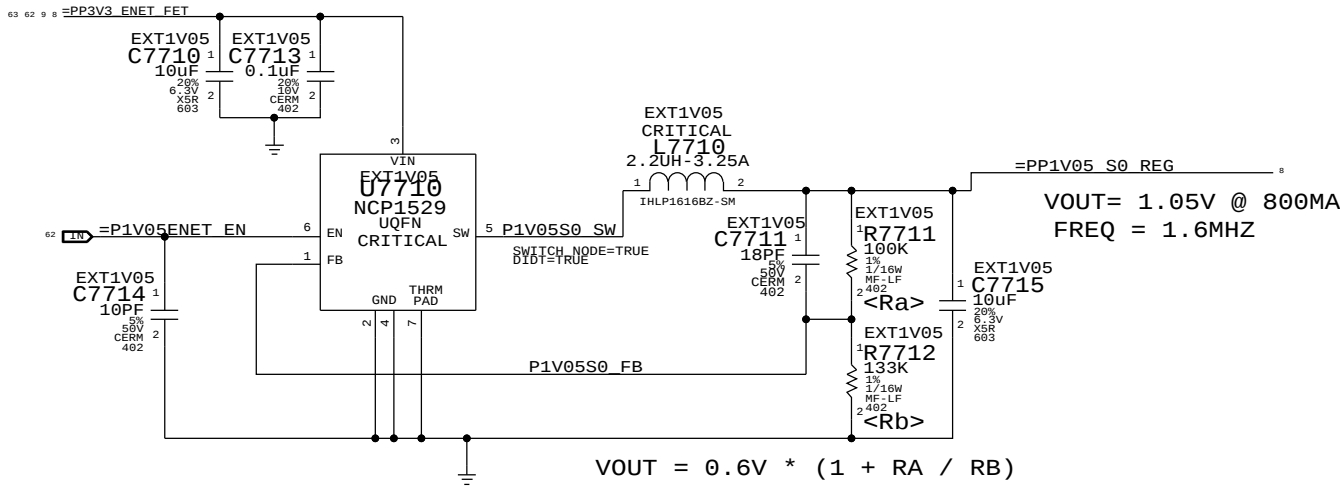
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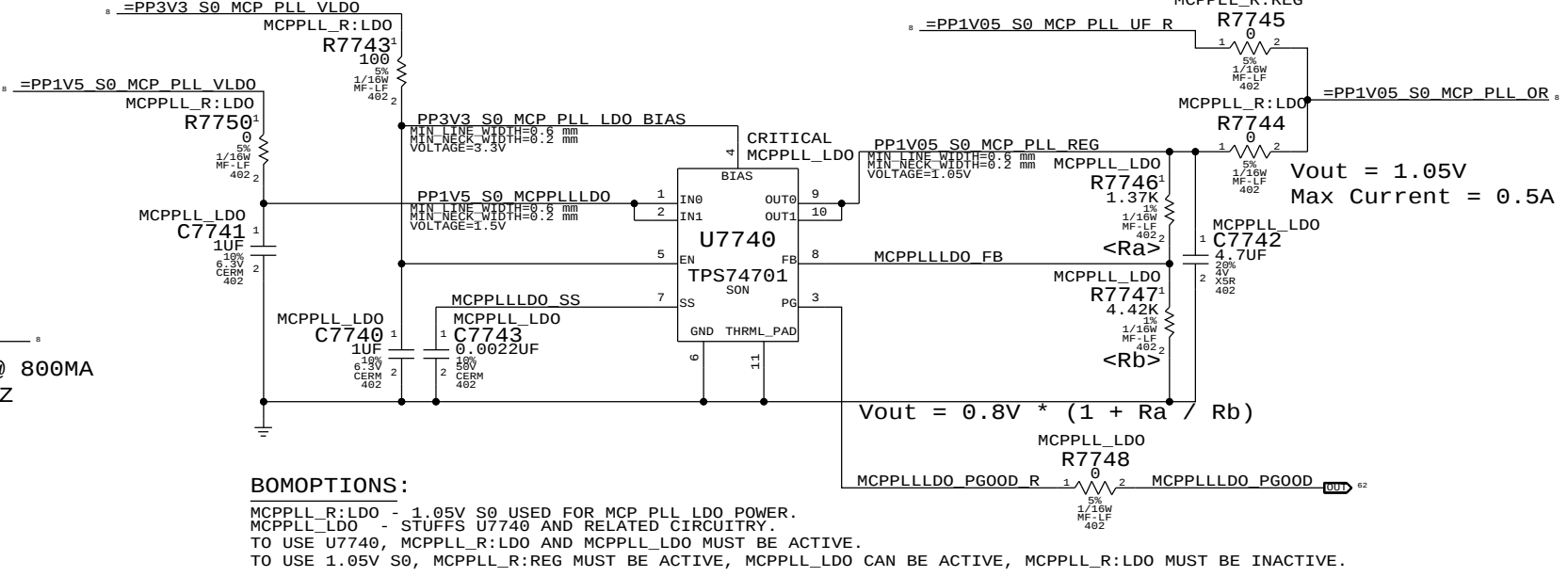
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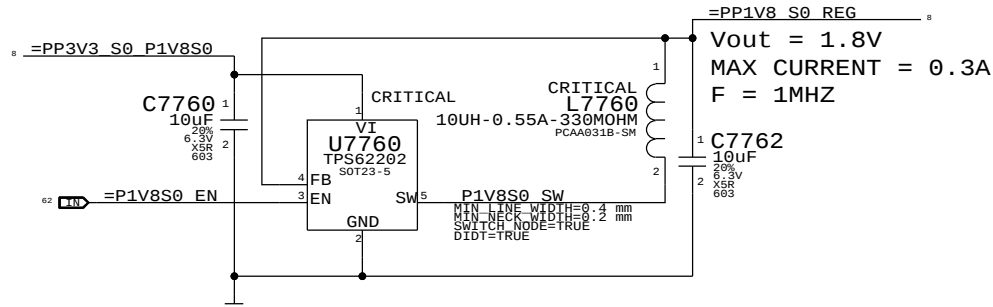
1.05V ENET Switcher



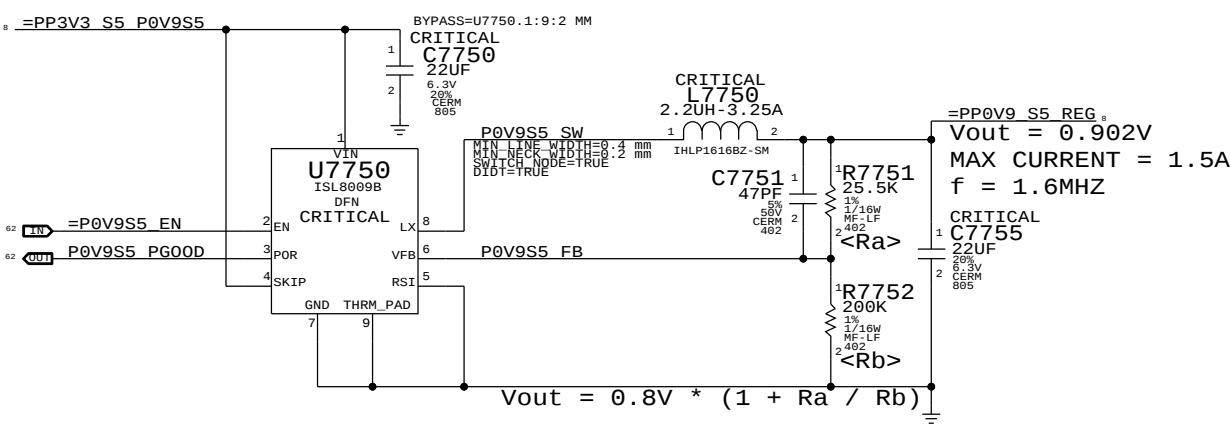
1.05V S0 MCP PLL LDO



1.8V S0 Switcher



MCP 0.9V S5 (AUXC) Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
Misc Power Supplies			
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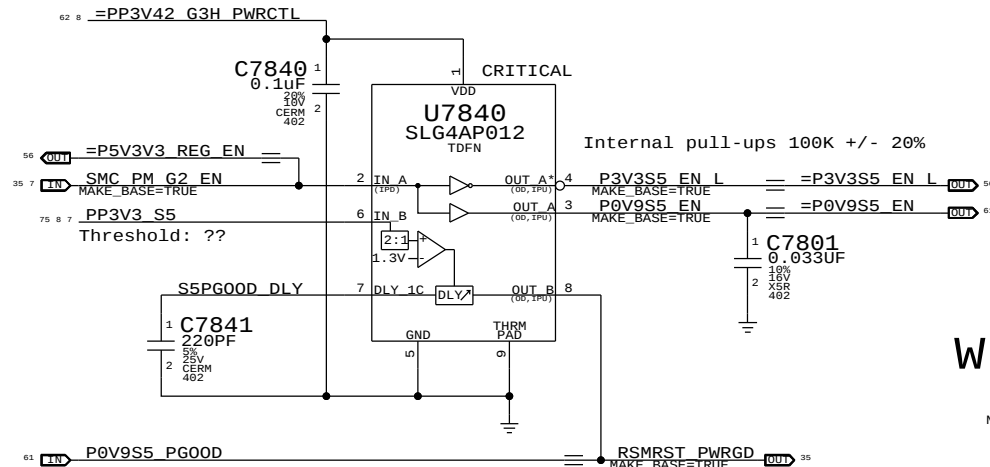
4

3

2

1

S5 Rail Enables & PG00D

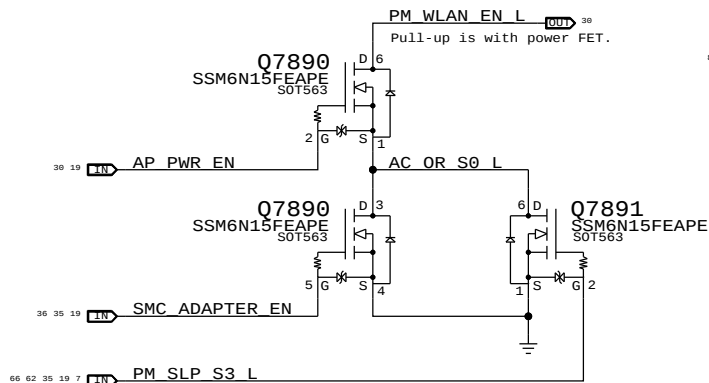


Power Control Signals

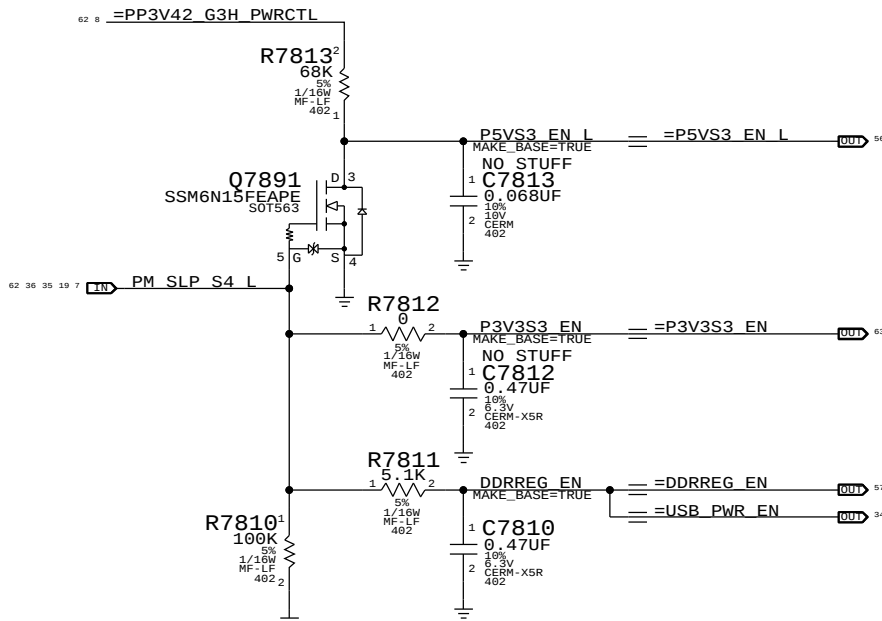
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

WLAN Enable Generation

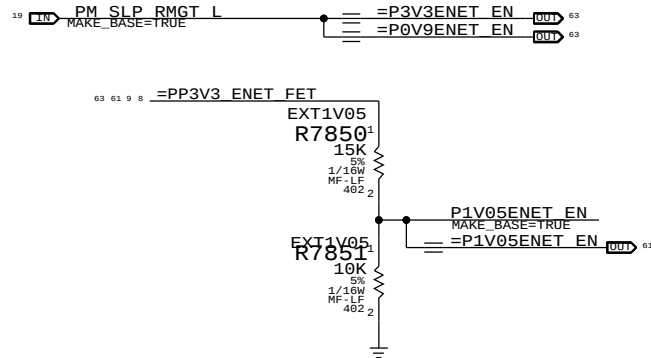
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



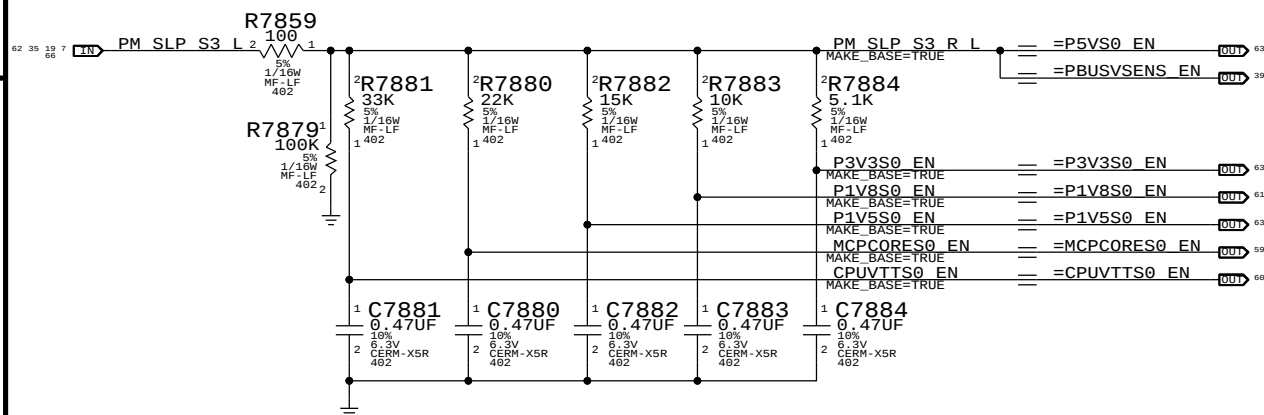
S3 Rail Enables



ENET Rail Enables



S0 Rail Enables

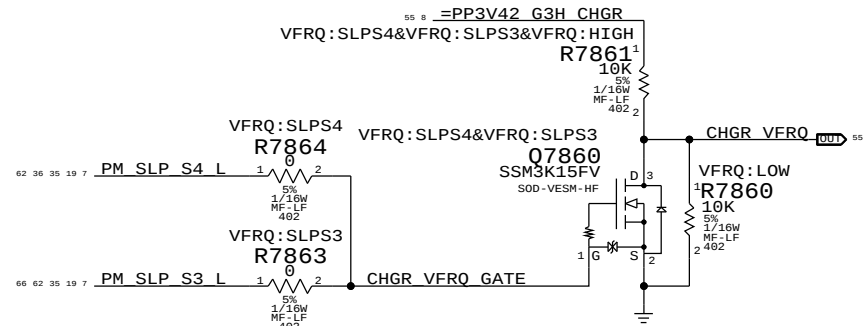


VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

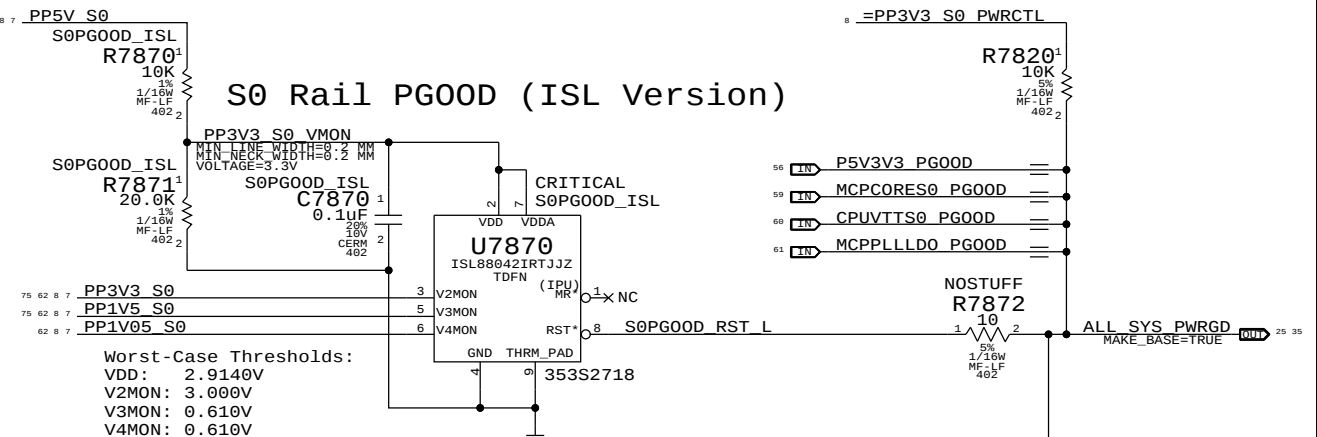
DO NOT SYNC T27, ENET RAILS CHANGED

ISL6259 Frequency Select

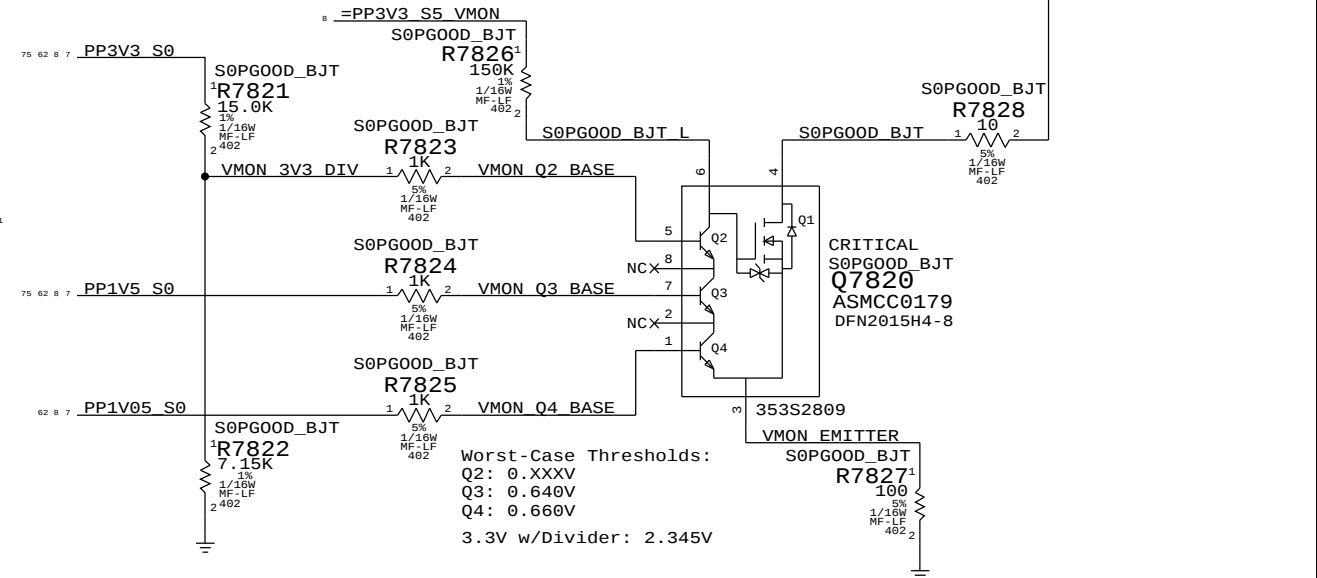


S0 Rail PG00D Circuitry

S0 Rail PG00D (ISL Version)



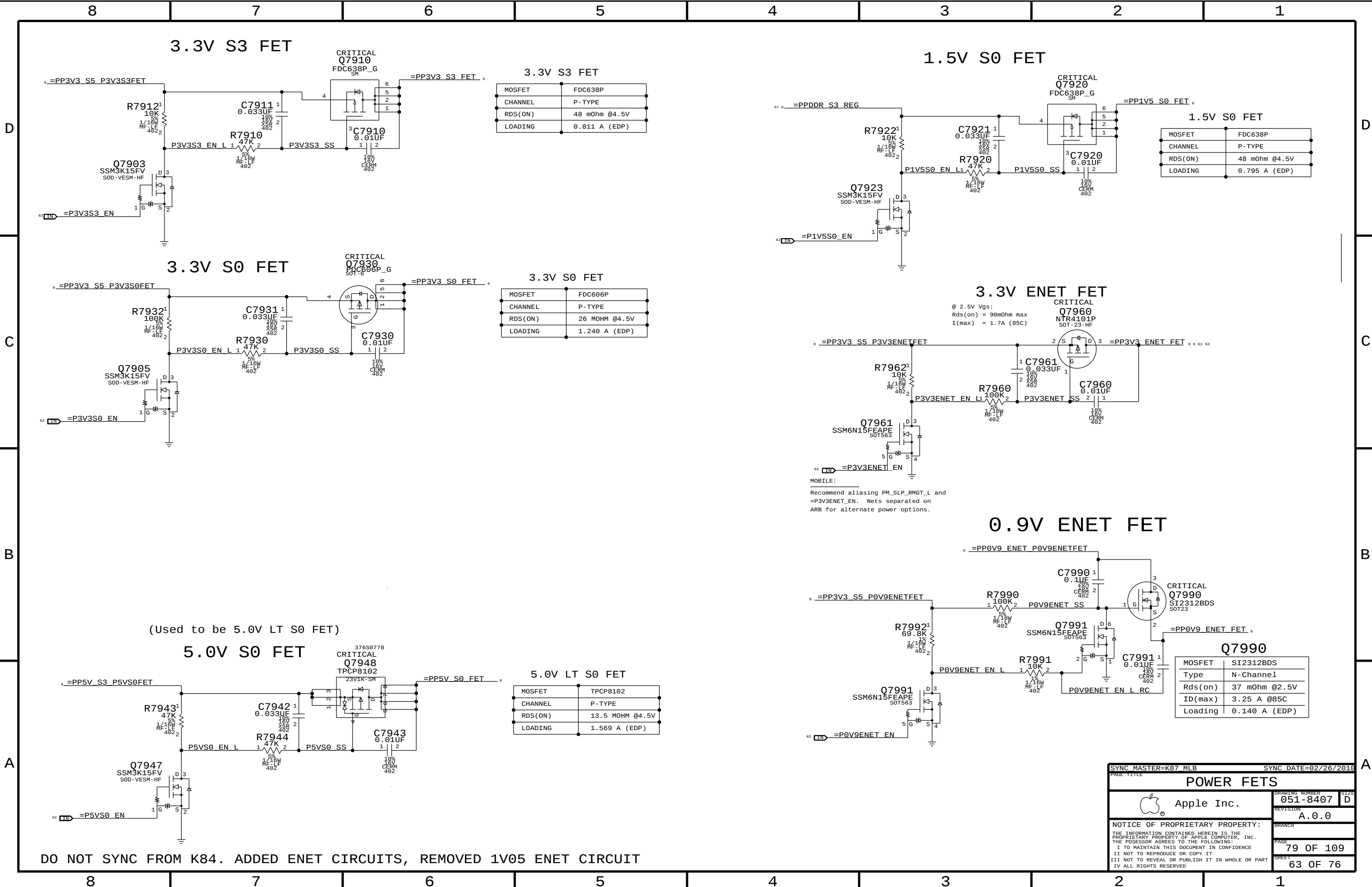
S0 Rail PG00D (BJT Version)



Unused PG00D signal

DDRREG_PG00D = TP_DDRREG_PG00D

SYNC_MASTER=K87_MLB		SYNC_DATE=02/26/2016	
PAGE TITLE			
Power Sequencing			
Apple Inc.		DRAWING NUMBER	051-8407
		REVISION	A.0.0
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BRANCH		PAGE	78 OF 109
SHEET		62 OF 76	



MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.811 A (EDP)

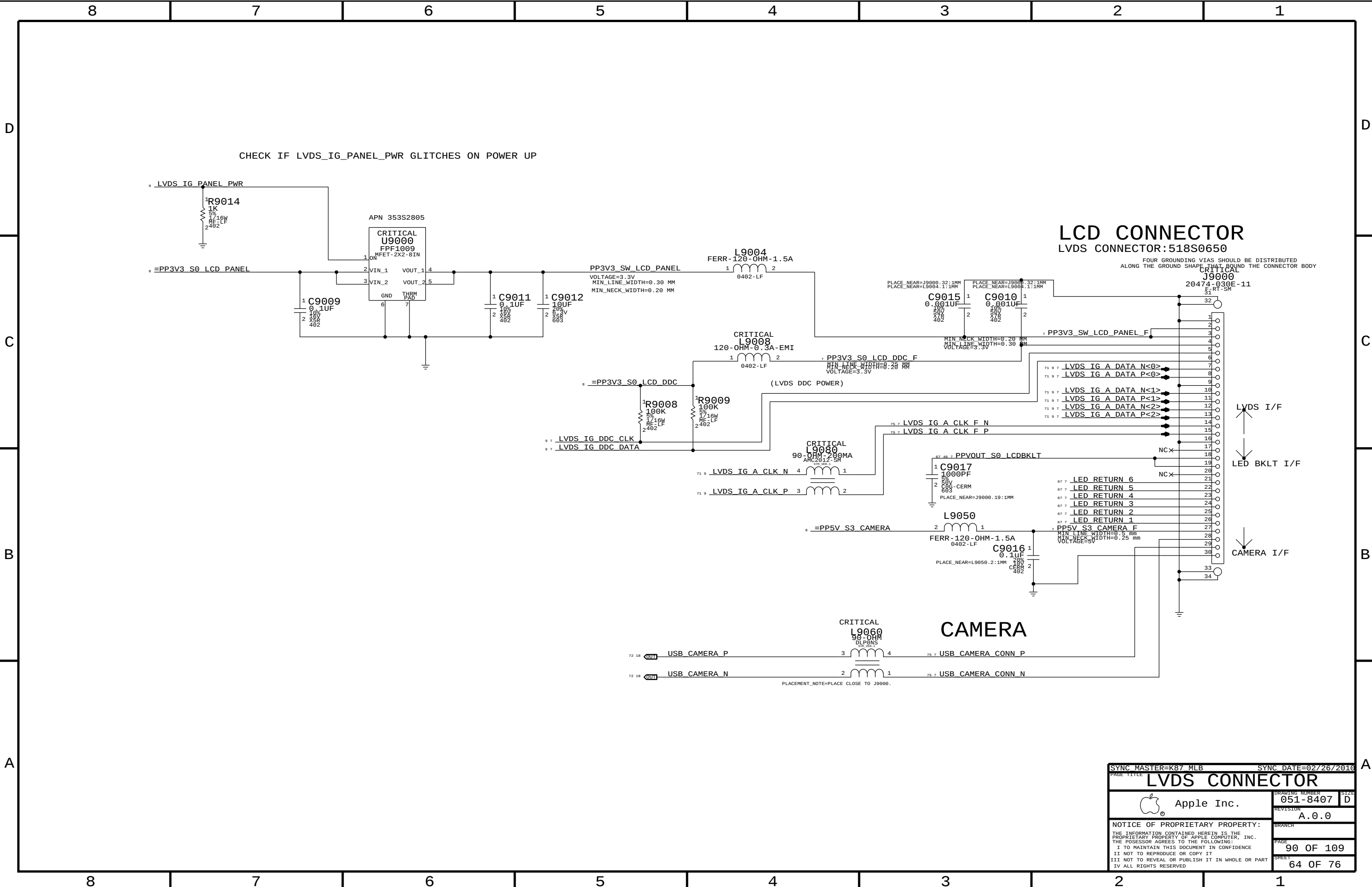
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.240 A (EDP)

MOSFET	NTR4101P
CHANNEL	N-TYPE
RDS(ON)	90mOhm max
I(max)	1.7A (85C)

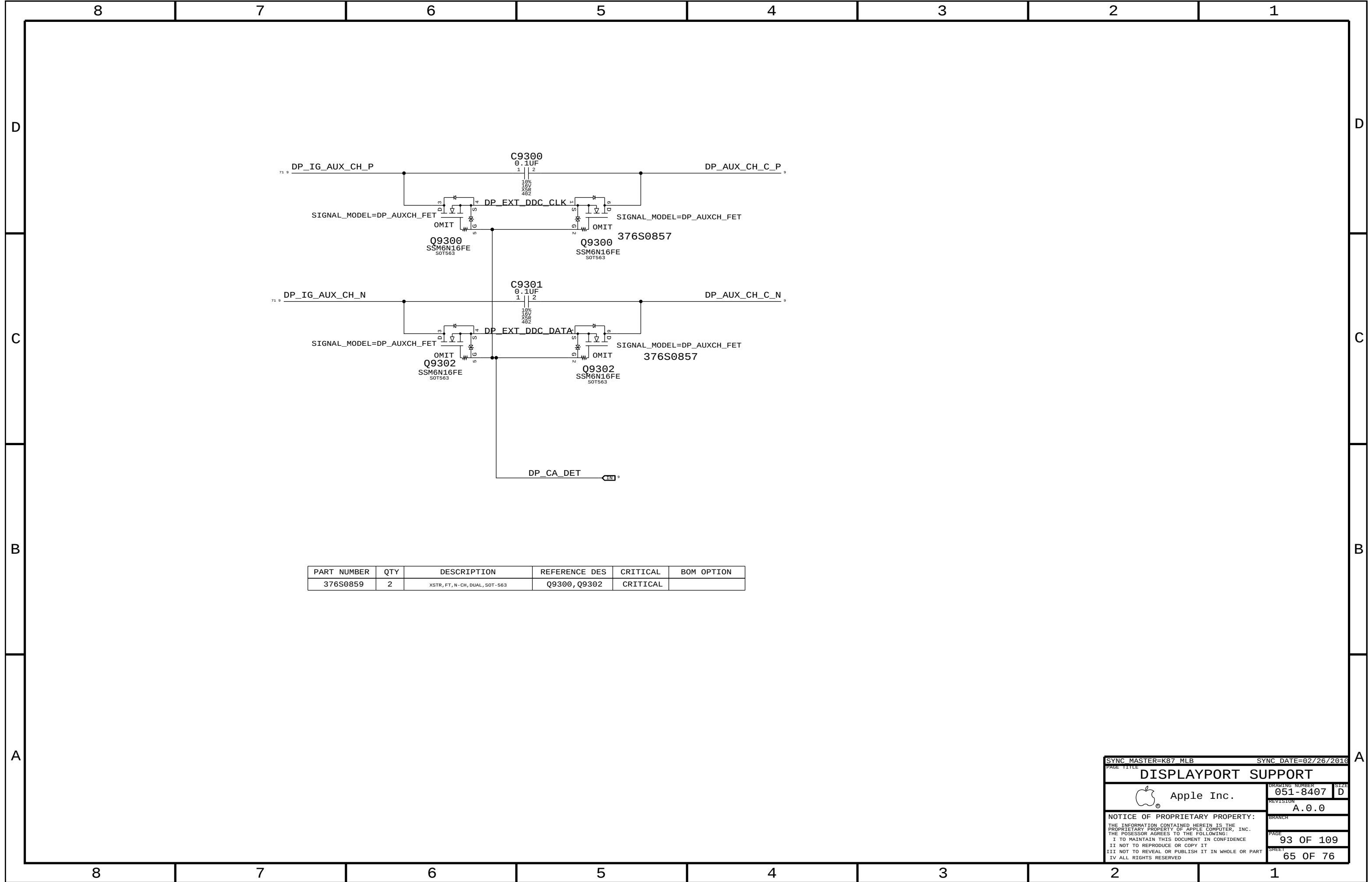
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

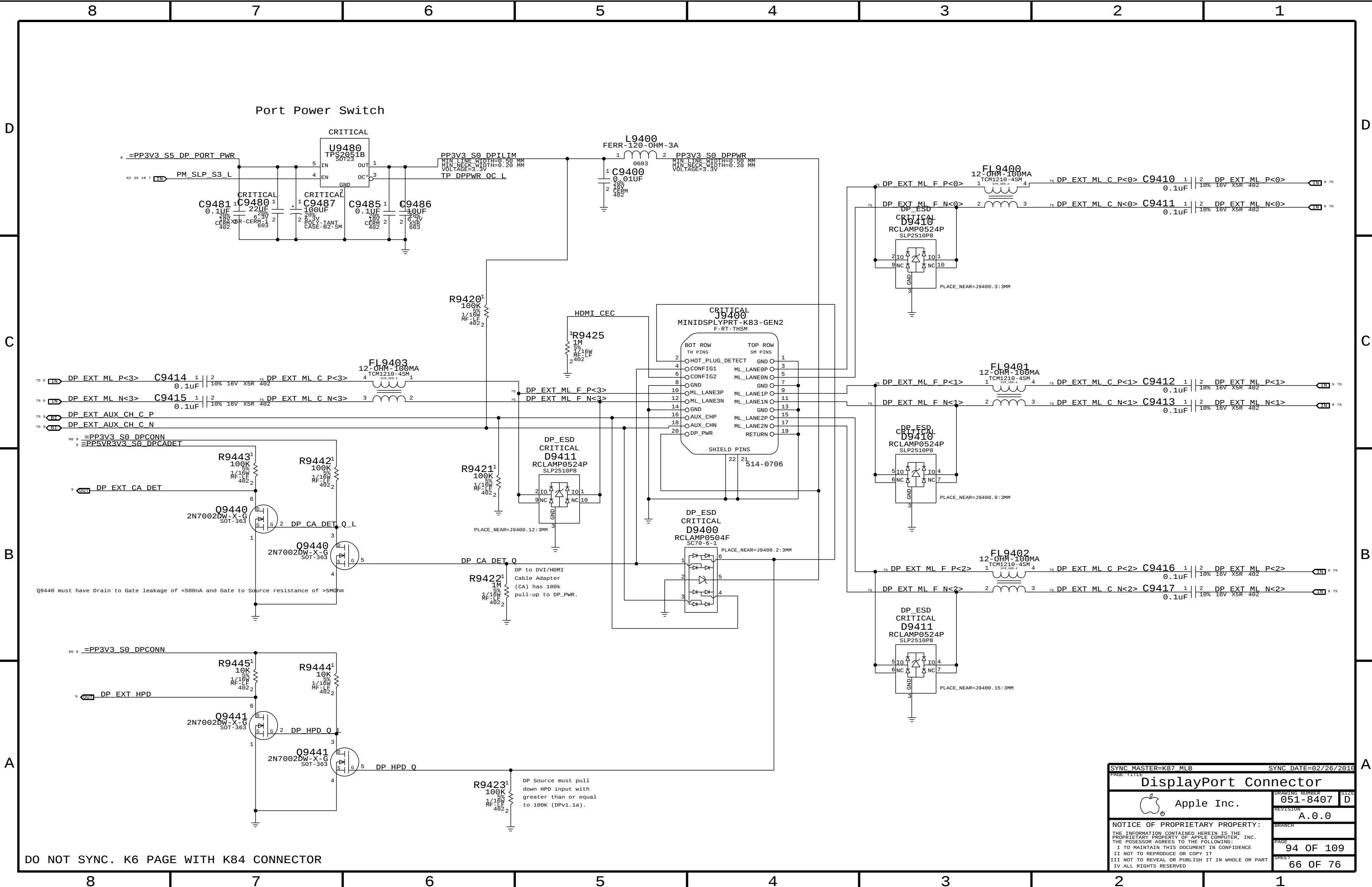
SYNC MASTER=K87_MLB		SYNC DATE=02/26/2016	
PAGE TITLE		POWER FETS	
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PAGE TITLE		LVDS CONNECTOR	
DRAWING NUMBER		051-8407	SIZE D
REVISION		A.0.0	BRANCH
PAGE		90 OF 109	SHEET
64 OF 76			

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SYNC_DATE=02/26/2016

DisplayPort Connector

 Apple Inc.

DRAWING NUMBER
051-8407

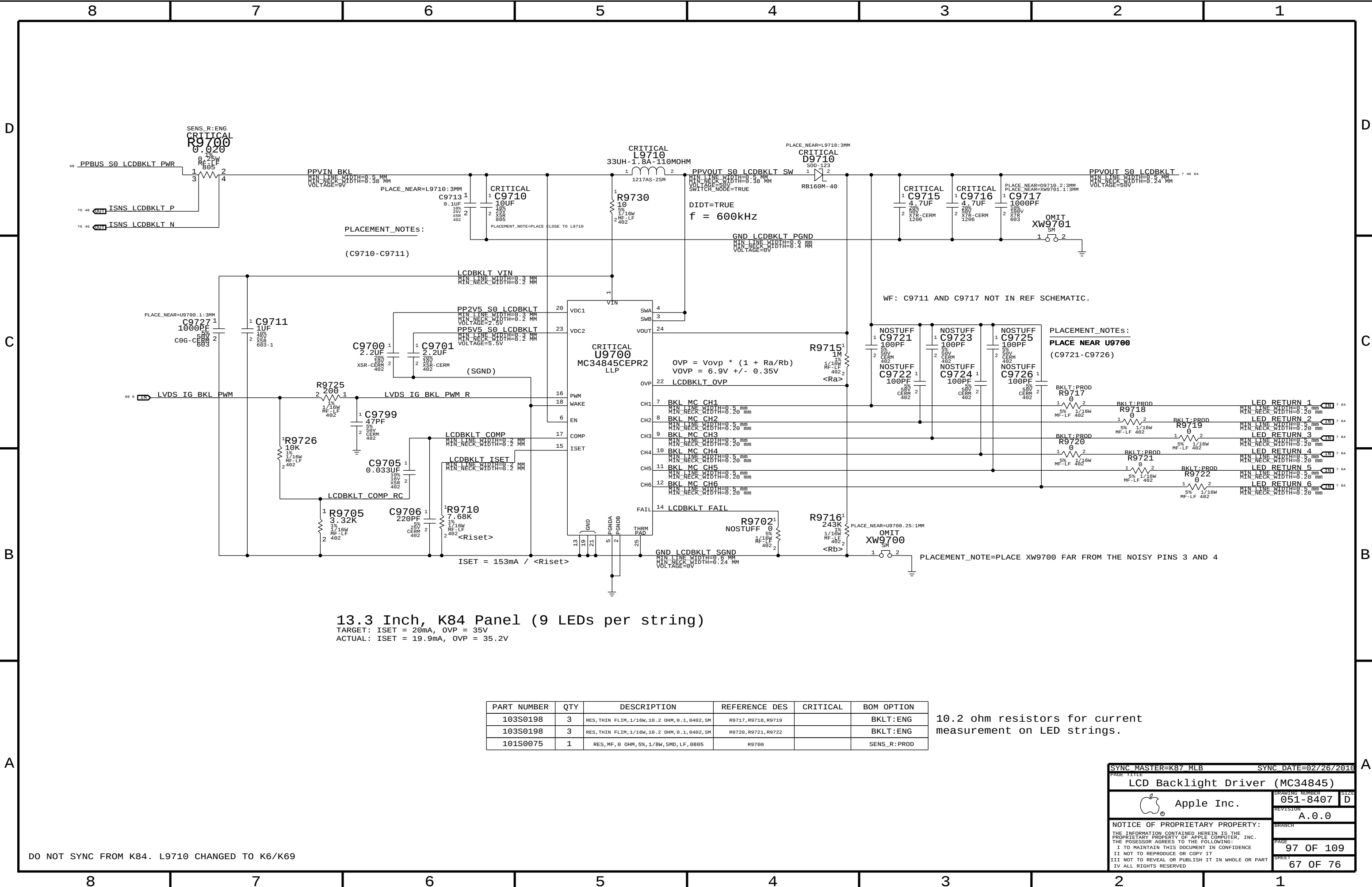
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DO NOT SYNC. K6 PAGE WITH K84 CONNECTOR



13.3 Inch, K84 Panel (9 LEDs per string)

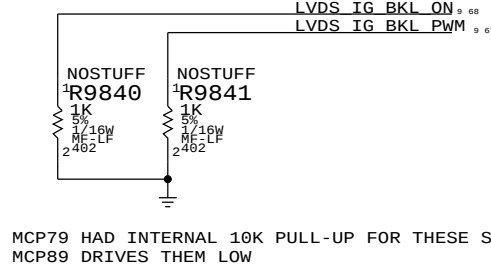
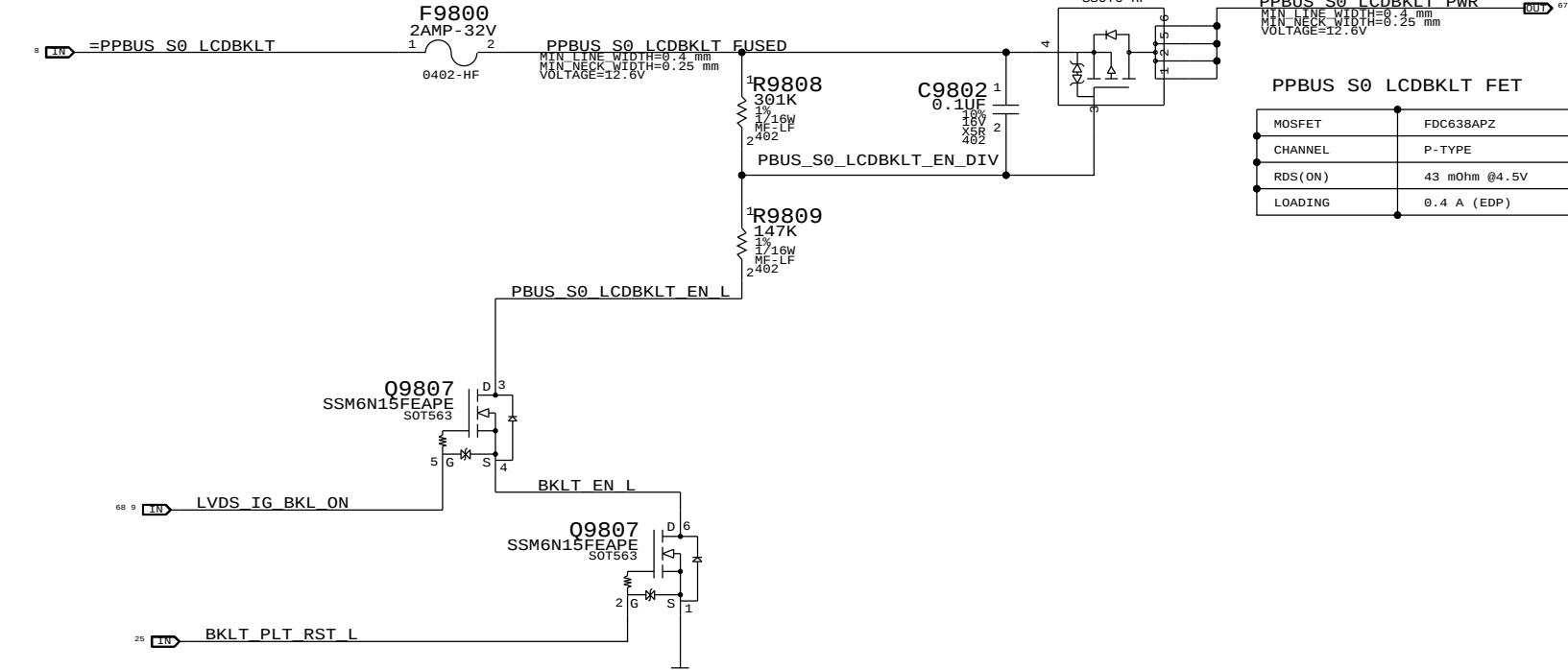
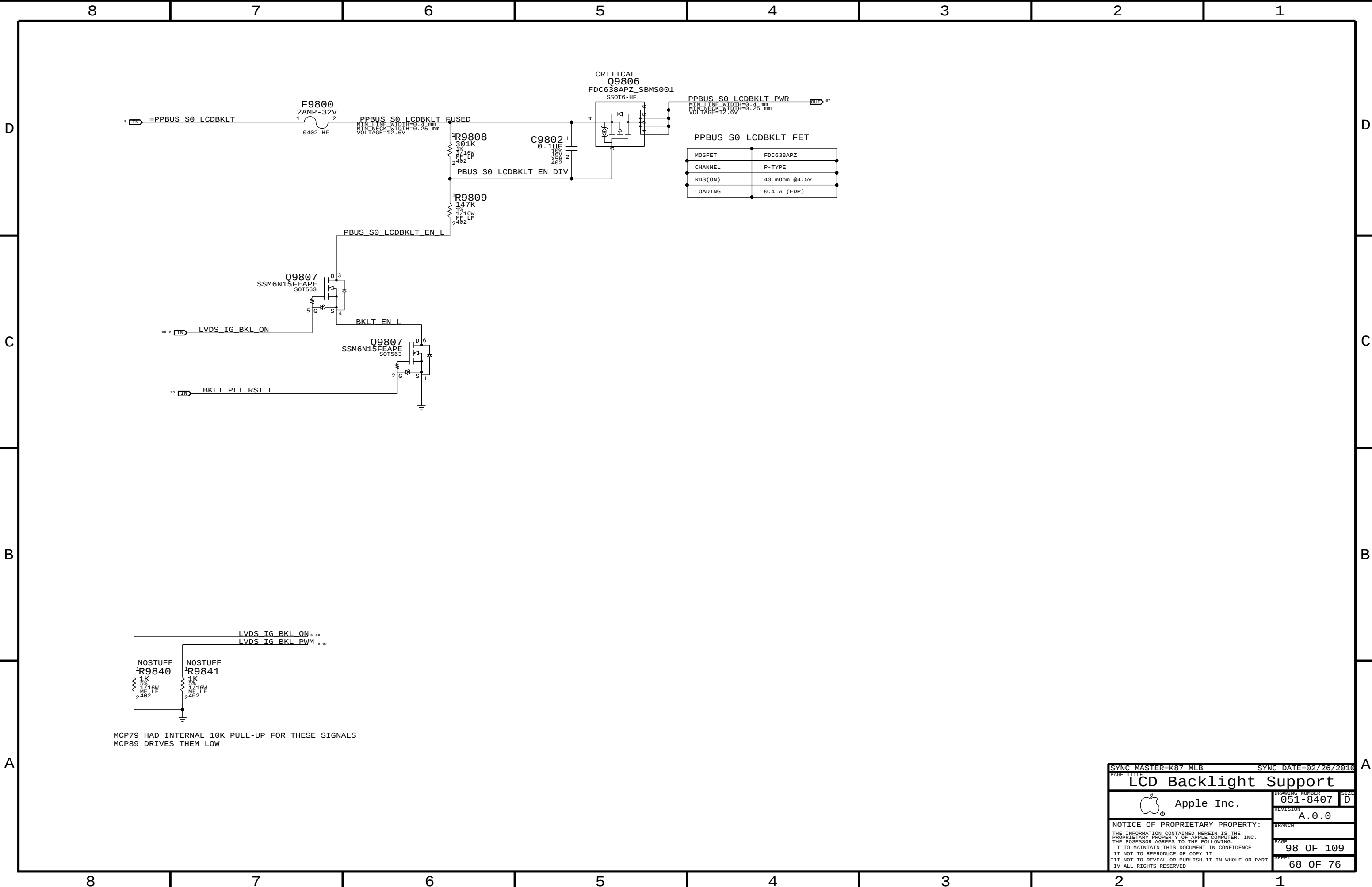
TARGET: ISET = 20mA, OVP = 35V
ACTUAL: ISET = 19.9mA, OVP = 35.2V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9720, R9721, R9722		BKLT:ENG
101S0075	1	RES, MF, 0 OHM, 5%, 1/8W, SMD, LF, 0805	R9700		SENS_R: PROD

10.2 ohm resistors for current measurement on LED strings.

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

SYNC MASTER=K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
LCD Backlight Driver (MC34845)			
 Apple Inc.	DRAWING NUMBER	051-8407	SIZE
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	25 MIL	?

NV DG says 3x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM	MEM_CLK	*	*	MEM_20THER
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM	MEM_CTRL	*	*	MEM_20THER
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM	MEM_CMD	*	*	MEM_20THER
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM	MEM_DATA	*	*	MEM_20THER
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM	MEM_DQS	*	*	MEM_20THER

DDR3: Need to support MEM_*-style wildcards!
DQS signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps.
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	15 26
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	15 26
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>	15 21 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A CS_L<3..0>	15 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE_L	15 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	15 27
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>	15 21 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B CS_L<3..0>	15 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE_L	15 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM_COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM_COMP GND	15

SYNC MASTER-K87 MLB		SYNC DATE=02/26/2016	
PAGE TITLE			
Memory Constraints			
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		REVISION	A.0.0
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4X_DIELECTRIC	?
MCP_DAC_COMP	*	=2X_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SATA	*	=3X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_R2D_N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>
PCIE_AP_D2R	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>
PCIE_ENET_R2D	PCIE_90D	PCIE	PEG_D2R_P<15..0>
PCIE_ENET_D2R	PCIE_90D	PCIE	PEG_D2R_N<15..0>
PCIE_FW_R2D	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>
PCIE_FW_D2R	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>
MCP_PEG_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE_AP_R2D_P
MCP_PE1_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE_AP_R2D_N
MCP_PE2_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE_AP_R2D_C_P
MCP_PE3_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE_AP_R2D_C_N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	PCIE_AP_D2R_P
CRT_RED	CRT_50S	CRT	PCIE_AP_D2R_N
CRT_GREEN	CRT_50S	CRT	PCIE_ENET_R2D_P
CRT_BLUE	CRT_50S	CRT	PCIE_ENET_R2D_N
CRT_SYNC	CRT_50S	CRT_SYNC	PCIE_ENET_R2D_C_P
MCP_DAC_RSET		MCP_DAC_COMP	PCIE_ENET_R2D_C_N
MCP_DAC_VREF		MCP_DAC_COMP	PCIE_ENET_D2R_P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	PCIE_ENET_D2R_N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	PCIE_ENET_D2R_C_P
TMDS_IG_TXD	DP_90D	DISPLAYPORT	PCIE_ENET_D2R_C_N
DP_EXT_ML	DP_90D	DISPLAYPORT	PCIE_FW_R2D_P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	PCIE_FW_R2D_N
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	PCIE_FW_R2D_C_P
MCP_TMDS0_RSET	MCP_DV_COMP		PCIE_FW_R2D_C_N
MCP_TMDS0_VPROBE			PCIE_FW_D2R_P
LVDS_IG_A_CLK	LVDS_100D	LVDS	PCIE_FW_D2R_N
LVDS_IG_A_CLK	LVDS_100D	LVDS	PCIE_FW_D2R_C_P
LVDS_IG_A_DATA	LVDS_100D	LVDS	PCIE_FW_D2R_C_N
LVDS_IG_A_DATA	LVDS_100D	LVDS	MCP_CLK100M_P
LVDS_IG_A_DATA3	LVDS_100D	LVDS	MCP_CLK100M_N
LVDS_IG_A_DATA3	LVDS_100D	LVDS	PCIE_CLK100M_AP_P
LVDS_IG_B_CLK	LVDS_100D	LVDS	PCIE_CLK100M_AP_N
LVDS_IG_B_CLK	LVDS_100D	LVDS	PCIE_CLK100M_ENET_P
LVDS_IG_B_DATA	LVDS_100D	LVDS	PCIE_CLK100M_ENET_N
LVDS_IG_B_DATA	LVDS_100D	LVDS	PCIE_CLK100M_FW_P
LVDS_IG_B_DATA3	LVDS_100D	LVDS	PCIE_CLK100M_FW_N
LVDS_IG_B_DATA3	LVDS_100D	LVDS	MCP_PEX0_TERM
MCP_IFPAB_RSET	MCP_DV_COMP		CRT_IG_R_C_PR
MCP_IFPAB_VPROBE			CRT_IG_G_Y_Y
SATA_HDD_R2D	SATA_90D	SATA	CRT_IG_B_COMP_PB
SATA_HDD_R2D	SATA_90D	SATA	CRT_IG_HSYNC
SATA_HDD_R2D	SATA_90D	SATA	CRT_IG_VSYNC
SATA_HDD_D2R	SATA_90D	SATA	MCP_TV_DAC_RSET
SATA_HDD_D2R	SATA_90D	SATA	MCP_TV_DAC_VREF
SATA_ODD_R2D	SATA_90D	SATA	TMDS_IG_TXC_P
SATA_ODD_R2D	SATA_90D	SATA	TMDS_IG_TXC_N
SATA_ODD_D2R	SATA_90D	SATA	TMDS_IG_TXD_P<5..0>
SATA_ODD_D2R	SATA_90D	SATA	TMDS_IG_TXD_N<5..0>
SATA_ODD_D2R	SATA_90D	SATA	DP_IG_ML_P<3..0>
SATA_ODD_D2R	SATA_90D	SATA	DP_IG_ML_N<3..0>
SATA_ODD_D2R	SATA_90D	SATA	DP_IG_AUX_CH_P
SATA_ODD_D2R	SATA_90D	SATA	DP_IG_AUX_CH_N
MCP_SATA_TERM		SATA_TERM	MCP_TMDS0_RSET

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SYNC_MASTER=K87_MLB

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MCP Constraints 1

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP, BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 35 37
	LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 35 37
	LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26
	MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
		CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 35
		CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	25 37
	USB_EXT_A	USR_90D	USR	USB_EXT_A_P	18 34
		USR_90D	USR	USB_EXT_A_N	18 34
		USR_90D	USR	USB_EXT_A_MUXED_P	34 75
		USR_90D	USR	USB_EXT_A_MUXED_N	34 75
	USB_MINI_T	USR_90D	USR	USB_MINI_P	9 18
		USR_90D	USR	USB_MINI_N	9 18
	USB_EXTD	USR_90D	USR	USB_EXTD_P	9 18
		USR_90D	USR	USB_EXTD_N	9 18
	USB_CAMERA	USR_90D	USR	USB_CAMERA_P	18 64
		USR_90D	USR	USB_CAMERA_N	18 64
	USB_BT	USR_90D	USR	USB_BT_P	18 30
		USR_90D	USR	USB_BT_N	18 30
	USB_TPAD	USR_90D	USR	USB_TPAD_P	18 43
		USR_90D	USR	USB_TPAD_N	18 43
	USB_IR	USR_90D	USR	USB_IR_P	9 18
		USR_90D	USR	USB_IR_N	9 18
	USB_EXTR	USR_90D	USR	USB_EXTR_P	18 34
		USR_90D	USR	USB_EXTR_N	18 34
	USB_T57	USR_90D	USR	USB_T57_P	9 18
		USR_90D	USR	USB_T57_N	9 18
	USB_EXTC	USR_90D	USR	USB_EXTC_P	9 18
		USR_90D	USR	USB_EXTC_N	9 18
	USB_SDCARD	USR_90D	USR	USB_SDCARD_P	9 18
		USR_90D	USR	USB_SDCARD_N	9 18
	USB_WM	USR_90D	USR	USB_WM_P	9 18
		USR_90D	USR	USB_WM_N	9 18
	MCP_USB_RBIA5	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	18
	SMBUS_MCP_0_CLK	SMR_55S	SMR	SMBUS_MCP_0_CLK	19 39 38
	SMBUS_MCP_0_DATA	SMR_55S	SMR	SMBUS_MCP_0_DATA	19 39 38
	(SMBUS_SMC_MGMT_SCL)	SMR_55S	SMR	SMBUS_MCP_1_CLK	19 38
	(SMBUS_SMC_MGMT_SDA)	SMR_55S	SMR	SMBUS_MCP_1_DATA	19 38
	HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	19 48
		HDA_55S	HDA	HDA_BIT_CLK_R	19
	HDA_SYNC	HDA_55S	HDA	HDA_SYNC	19 48
		HDA_55S	HDA	HDA_SYNC_R	19
	HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	19
		HDA_55S	HDA	HDA_RST_L	19 48
	HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	19 48
		HDA_55S	HDA	HDA_SDIN_CODEC	48
	HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	19 48
		HDA_55S	HDA	HDA_SDOUT_R	19
	MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	19
	MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	19 26
		CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 35
	SPI_CLK	SPT_55S	SPT	SPI_CLK_R	19 37
		SPT_55S	SPT	SPI_CLK	7 37
	SPI_MOSI	SPT_55S	SPT	SPI_MOSI_R	19 37
		SPT_55S	SPT	SPI_MOSI	7 37
	SPI_MISO	SPT_55S	SPT	SPI_MISO	7 19 37
	SPI_CS0	SPT_55S	SPT	SPI_CS0_R_L	19 37
		SPT_55S	SPT	SPI_CS0_L	7 37
		SPT_55S	SPT	SPI_MLB_CLK	37 47
		SPT_55S	SPT	SPI_MLB_MOSI	37 47
		SPT_55S	SPT	SPI_MLB_MISO	37 47
		SPT_55S	SPT	SPI_MLB_CS_L	37 47
		SPT_55S	SPT	SPI_ALT_CLK	37
		SPT_55S	SPT	SPI_ALT_MOSI	37
		SPT_55S	SPT	SPI_ALT_MISO	37
		SPT_55S	SPT	SPI_ALT_CS_L	37

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NCP_M1L_COMP	*	==STANDARD	7.5 M1L	7.5 M1L	==STANDARD	==STANDARD	==STANDARD
ENET_M1L_55S	*	==55_OHM_SE	==55_OHM_SE	==55_OHM_SE	==55_OHM_SE	==STANDARD	==STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	"	=3:1_SPACING	?
ENET_MII	"	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

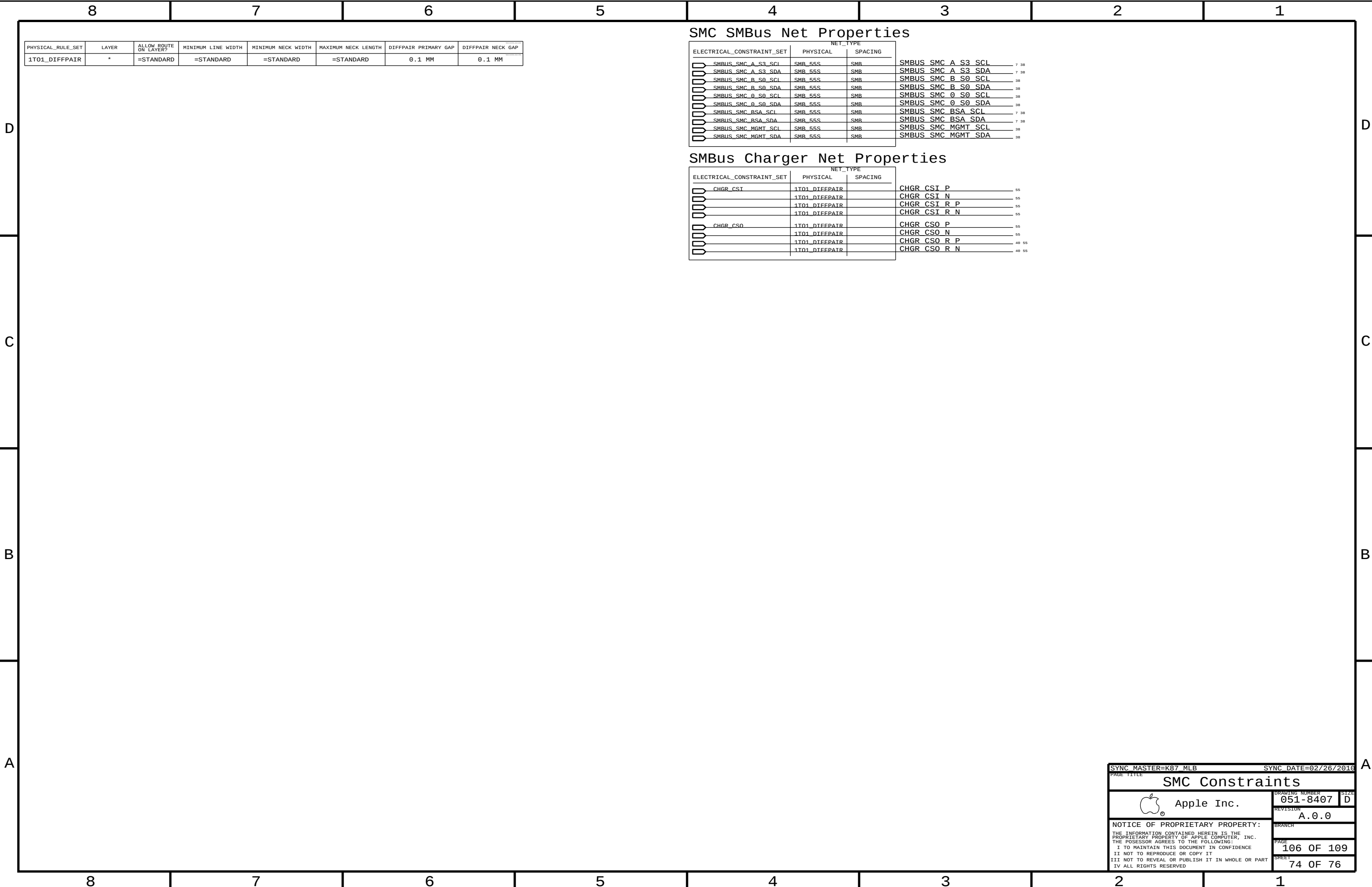
88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 18
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 18
	MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M_BUF0 R 9
		ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1 31
	ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L 18
	ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 18 31
	ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC 9 31
	ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L 18
		ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R 31
	ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 31
		ENET_MII_55S	ENET_MII	ENET_RXD R<3..0> 31
	ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0> 31
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 18 31
	ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 18 31
		ENET_MII_55S	ENET_MII	ENET_RXCTL R 31
		ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R 31
	ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK 31
	ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0> 9 31
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1> 9 31
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL 9 31
		ENET_MII_55S	ENET_MII	ENET_RESET_L 9 31
	ENET_MDI	ENET_MDI_1000	ENET_MDI	ENET_MDI P<3..0> 31 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI N<3..0> 31 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI_TRAN P<3..0> 31 32
		ENET_MDI_1000	ENET_MDI	ENET_MDI_TRAN N<3..0> 32



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PwR_P2MM
SATA	SB_POWER	*	PwR_P2MM
USB	SB_POWER	*	PwR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	(PCIE_AP)	CLK PCIE 100D	CLK PCIE	PCIE CLK100M AP CONN P
		CLK PCIE 100D	CLK PCIE	PCIE CLK100M AP CONN N
	(USB_EXT_A)	USB 90D	USB	USB_EXT_A MUXED P
	(USB_EXT_A)	USB 90D	USB	USB_EXT_A MUXED N
	(USB_EXT_A)	USB 90D	USB	USB LT1 P
	(USB_EXT_A)	USB 90D	USB	USB LT1 N
	(USB_TPAD)	USB 90D	USB	USB_TPAD R P
	(USB_TPAD)	USB 90D	USB	USB_TPAD R N
	(USB_CAMERA)	USB 90D	USB	USB_CAMERA CONN P
	(USB_CAMERA)	USB 90D	USB	USB_CAMERA CONN N
		USB 90D	USB	USB LT2 P
		USB 90D	USB	USB LT2 N
		ENET_MDT 100D	ENETCONN	ENETCONN P<3..0>
		ENET_MDT 100D	ENETCONN	ENETCONN N<3..0>
		SATA 90D	SATA	SATA_ODD_R2D_UF_P
		SATA 90D	SATA	SATA_ODD_R2D_UF_N
		SATA 90D	SATA	SATA_ODD_D2R_UF_P
		SATA 90D	SATA	SATA_ODD_D2R_UF_N
		SATA 90D	SATA	SATA_HDD_D2R_FILT_P
		SATA 90D	SATA	SATA_HDD_D2R_FILT_N
		SATA 90D	SATA	SATA_HDD_D2R_UF_P
		SATA 90D	SATA	SATA_HDD_D2R_UF_N
		SATA 90D	SATA	SATA_HDD_R2D_UF_P
		SATA 90D	SATA	SATA_HDD_R2D_UF_N
		SATA 90D	SATA	SATA_HDD_D2R_RDRV_IN_P
		SATA 90D	SATA	SATA_HDD_D2R_RDRV_IN_N
		SATA 90D	SATA	SATA_HDD_R2D_RDRV_IN_P
		SATA 90D	SATA	SATA_HDD_R2D_RDRV_IN_N
		SATA 90D	SATA	SATA_HDD_D2R_RDRV_OUT_P
		SATA 90D	SATA	SATA_HDD_D2R_RDRV_OUT_N
		SATA 90D	SATA	SATA_HDD_R2D_RDRV_OUT_P
		SATA 90D	SATA	SATA_HDD_R2D_RDRV_OUT_N
		SATA 90D	SATA	SATA_HDD_D2R_NORDRV_P
		SATA 90D	SATA	SATA_HDD_D2R_NORDRV_N
		SATA 90D	SATA	SATA_HDD_R2D_NORDRV_P
		SATA 90D	SATA	SATA_HDD_R2D_NORDRV_N
	PCIE_AP_D2R	PCIE 90D	PCIE	CONN PCIE MINI D2R P
		PCIE 90D	PCIE	CONN PCIE MINI D2R N
	PCIE_AP_R2D	PCIE 90D	PCIE	CONN PCIE MINI R2D P
		PCIE 90D	PCIE	CONN PCIE MINI R2D N
	USB_BT	USB 90D	USB	CONN USB2_BT_P
		USB 90D	USB	CONN USB2_BT_N
	LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P
		LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N
	MCP_PE1_REFCLK	CLK PCIE 100D	CLK PCIE	PCIE CLK100M MINI CONN P
		CLK PCIE 100D	CLK PCIE	PCIE CLK100M MINI CONN N
USB	USB_EXT_A	USB 90D	USB	CONN USB_EXT_A_P
USB		USB 90D	USB	CONN USB_EXT_A_N
USB	USB_EXT_B	USB 90D	USB	CONN USB_EXT_B_P
USB		USB 90D	USB	CONN USB_EXT_B_N

Power Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CPU1THMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D1 P 41
		THERM_1T01_55S	THERM	CPUTHMSNS D1 N 41
100	CPU1THMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D2 P 41
100		THERM_1T01_55S	THERM	CPUTHMSNS D2 N 41
	CPU1THERMD	THERM_1T01_55S	THERM	CPU1THERMD P 10 41
		THERM_1T01_55S	THERM	CPU1THERMD N 10 41
	MCPTHMSNS_D2	THERM_1T01_55S	THERM	MCPTHMSNS D2 P
		THERM_1T01_55S	THERM	MCPTHMSNS D2 N
	MCP1THMDIODE	THERM_1T01_55S	THERM	MCP1THMDIODE P 19 41
		THERM_1T01_55S	THERM	MCP1THMDIODE N 19 41
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1V5 S3 P
		SENSE_1T01_55S	SENSE	ISNS1V5 S3 N
		SENSE_1T01_55S	SENSE	ISNS1V5 S3 R P
		SENSE_1T01_55S	SENSE	ISNS1V5 S3 R N
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1AIRPORT P 30 46
		SENSE_1T01_55S	SENSE	ISNS1AIRPORT N 30 46
		SENSE_1T01_55S	SENSE	ISNS1AIRPORT R P 46
		SENSE_1T01_55S	SENSE	ISNS1AIRPORT R N 46
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1HDD P 33 46
		SENSE_1T01_55S	SENSE	ISNS1HDD N 33 46
		SENSE_1T01_55S	SENSE	ISNS1HDD R P 46
		SENSE_1T01_55S	SENSE	ISNS1HDD R N 46
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1LCDBKLT P 46 67
		SENSE_1T01_55S	SENSE	ISNS1LCDBKLT N 46 67
		SENSE_1T01_55S	SENSE	ISNS1LCDBKLT R P
		SENSE_1T01_55S	SENSE	ISNS1LCDBKLT R N
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1ODD P 33 46
		SENSE_1T01_55S	SENSE	ISNS1ODD N 33 46
		SENSE_1T01_55S	SENSE	ISNS1ODD R P 46
		SENSE_1T01_55S	SENSE	ISNS1ODD R N 46
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	ISNS1CPUVTT P 40
		SENSE_1T01_55S	SENSE	ISNS1CPUVTT N 40
	SENSE1DIEFPATR	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN P 22 59
		SENSE_1T01_55S	SENSE	MCPCORES0 VSEN N 22 59
100		MEM_POWER		PP1V5R1V35 S3 7 8
		SB_POWER		PP3V3 S5 7 8 62
		SB_POWER		PP3V3 S0 7 8 62
		SB_POWER		PP1V5 S0 7 8 62
		GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DIEFPATR	AUDIO	AUD SPKRAMP LIN P
		DIEFPATR	AUDIO	AUD SPKRAMP LIN N
		DIEFPATR	AUDIO	AUD SPKRAMP SUBIN P
		DIEFPATR	AUDIO	AUD SPKRAMP SUBIN N
		DIEFPATR	AUDIO	AUD SPKRAMP RIN P
		DIEFPATR	AUDIO	AUD SPKRAMP RIN N
		DIEFPATR	AUDIO	SSM2315L P
		DIEFPATR	AUDIO	SSM2315L N
		DIEFPATR	AUDIO	SSM2315S P
		DIEFPATR	AUDIO	SSM2315S N
		DIEFPATR	AUDIO	SSM2315R P
		DIEFPATR	AUDIO	SSM2315R N
	SPK_OUT	DIEFPATR	AUDIO	SPKRCONN L OUT P
		DIEFPATR	AUDIO	SPKRCONN L OUT N
	SPK_OUT	DIEFPATR	AUDIO	SPKRCONN S OUT P
		DIEFPATR	AUDIO	SPKRCONN S OUT N
	SPK_OUT	DIEFPATR	AUDIO	SPKRCONN R OUT P
		DIEFPATR	AUDIO	SPKRCONN R OUT N
		DIEFPATR	AUDIO	BI MIC P
		DIEFPATR	AUDIO	BI MIC N
		DIEFPATR	AUDIO	HS MIC P
		DIEFPATR	AUDIO	HS MIC N

GRAPHICS NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
(DP_FXT_ML)	DP_96D	DISPLAYPORT	DP EXT ML P<3..0>	9 66
	DP_96D	DISPLAYPORT	DP EXT ML N<3..0>	9 66
	DP_96D	DISPLAYPORT	DP EXT ML C P<3..0>	66
	DP_96D	DISPLAYPORT	DP EXT ML C N<3..0>	66
	DP_96D	DISPLAYPORT	DP EXT ML F P<3..0>	66
	DP_96D	DISPLAYPORT	DP EXT ML F N<3..0>	66
(DP_FXT_AUX_CH)	DP_96D	DISPLAYPORT	DP EXT AUX CH C P	9 66
	DP_96D	DISPLAYPORT	DP EXT AUX CH C N	9 66
	DP_96D	DISPLAYPORT	DP EXT DDC DATA	65
	DP_96D	DISPLAYPORT	DP EXT DDC CLK	65

SYNCH MASTER=K87 MLB		SYNCH DATE=02/26/2016	
PAGE TITLE			
K87 SPECIFIC CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER 051-8407	SIZE D
		REVISION A.0.0	
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K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (REL. OF MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P3MM		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
DEFAULT				*	0.50 MM	?	
STANDARD				*	=DEFAULT	?	
BGA_P1MM				*	=DEFAULT	?	
BGA_P2MM				*	=DEFAULT	?	
BGA_P3MM				*	=DEFAULT	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
1.5:1_SPACING				*	0.15 MM	?	
2:1_SPACING				*	0.2 MM	?	
2.5:1_SPACING				*	0.25 MM	?	
3:1_SPACING				*	0.3 MM	?	
4:1_SPACING				*	0.4 MM	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
1.5X_DIELECTRIC				TOP, BOTTOM	0.105 MM	?	
2X_DIELECTRIC				TOP, BOTTOM	0.140 MM	?	
3X_DIELECTRIC				TOP, BOTTOM	0.210 MM	?	
4X_DIELECTRIC				TOP, BOTTOM	0.280 MM	?	
5X_DIELECTRIC				TOP, BOTTOM	0.350 MM	?	
1.5X_DIELECTRIC				*	0.095 MM	?	
2X_DIELECTRIC				*	0.126 MM	?	
3X_DIELECTRIC				*	0.189 MM	?	
4X_DIELECTRIC				*	0.252 MM	?	
5X_DIELECTRIC				*	0.315 MM	?	
NET_SPACING_TYPE1				NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
*				*	BGA_P1MM	BGA_P1MM	
MEM_CLK				*	BGA_P1MM	BGA_P2MM	
CLK_FSB				*	BGA_P1MM	BGA_P2MM	
CLK_LPC				*	BGA_P1MM	BGA_P2MM	
CLK_PCIE				*	BGA_P1MM	BGA_P2MM	
CLK_SLOW				*	BGA_P1MM	BGA_P2MM	
FSB_DSTB				FSB_DSTB	BGA_P1MM	BGA_P3MM	
NET_PHYSICAL_TYPE				AREA_TYPE	PHYSICAL_RULE_SET		
MEM_485				BGA_P1MM	STANDARD		
SYNC_MASTER=K87_MLB SYNC_DATE=12/03/2009							
K87 RULE DEFINITIONS							
 Apple Inc.				DRAWING NUMBER	051-8407	SIZE	D
				REVISION	A.0.0		
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